

Model Name: GA-P35-S3 Rev1.02

SHEET TITLE

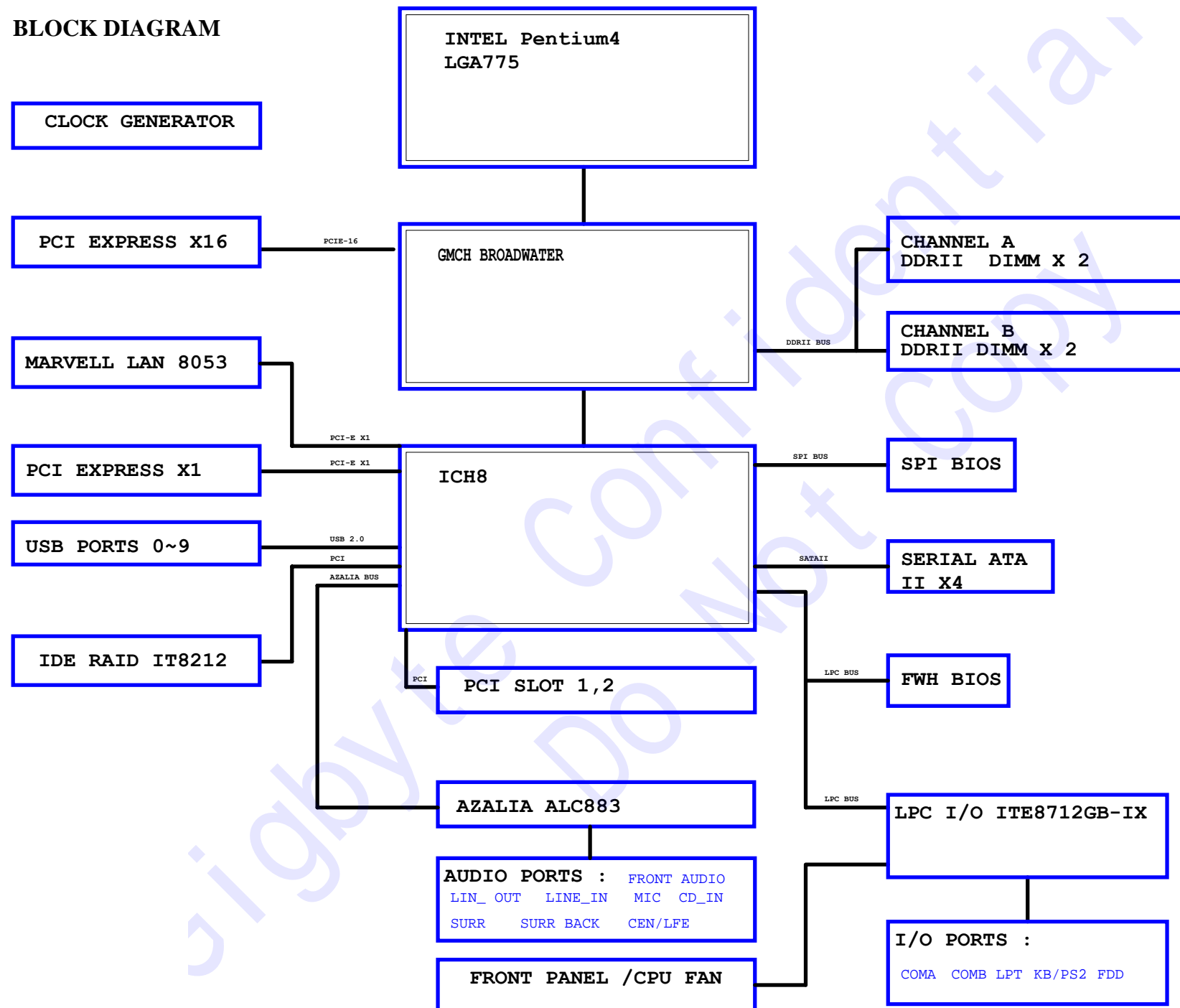
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	POWER MAP
05	P4 LGA775 A
06	P4 LGA775 B
07	P4 LGA775 C
08	P4 LGA775 D
09	GMCH-BEARLAKE HOST
10	GMCH-BEARLAKE DDRII
11	GMCH-BEARLAKE PCI E, DMI
12	GMCH-BEARLAKE INT VGA
13	GMCH-BEARLAKE GND
14	GMCH-BEARLAKE PWR
15	DDRII CHANNEL A 1,2
16	DDRII CHANNEL B 1,2
17	DDRII TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH9 PCI, USB, DMI, LAN
20	ICH9 GPIO, CTRL
21	ICH9 SATA, FAN PWM
22	ICH9 VCC, GND
23	CLOCK GEN CK505
24	PCI EXPRESS*1 ,PCI SLOT 1,2
25	ITE8718/GB,RESET DRIVE
26	COM,LPT
27	BIOS,CI,HWM,KB/MS

SHEET TITLE

28	AZALIA ALC889A
29	AUDIO JACK
30	VCORE PWM ISL6327
31	DISCRETE POWER
32	ATX POWER
33	JMicron JMB363
34	LAN REALTEK RTL8111B
35	FRONT PANEL,FUSB,FDD

Gigabyte Technology

Title		
Cover Sheet		
Size	Document Number	Rev
Custom	P35-S3	1.02
Date:	Wednesday, April 09, 2008	Sheet 1 of 35

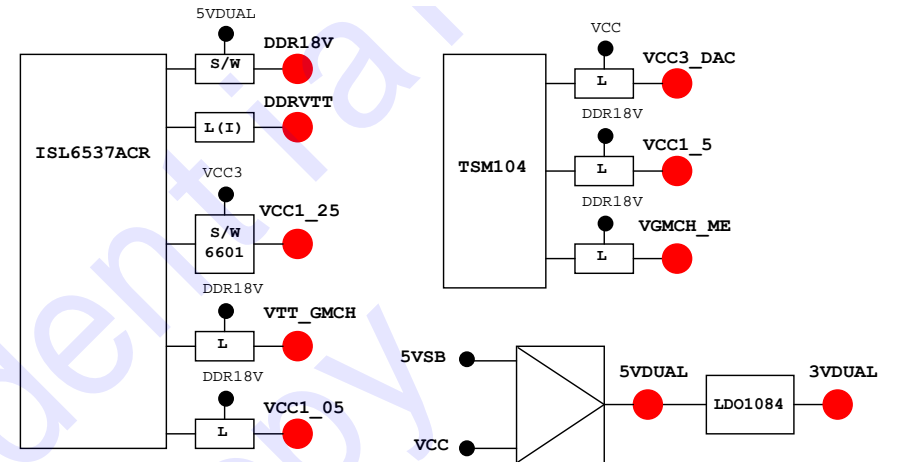
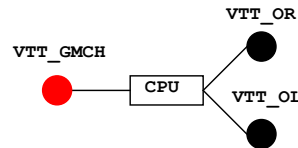
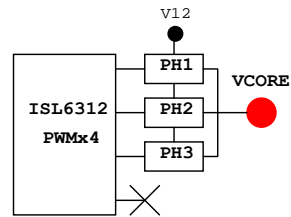
BLOCK DIAGRAM

Gigabyte Technology

ICH8 GPIO LIST TABLE

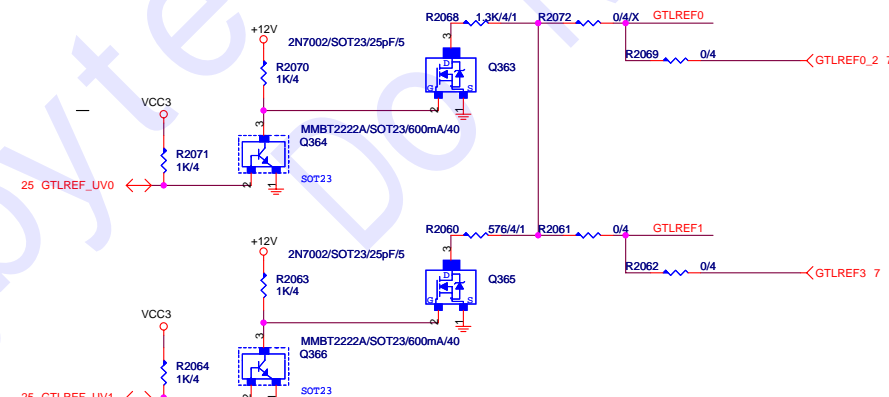
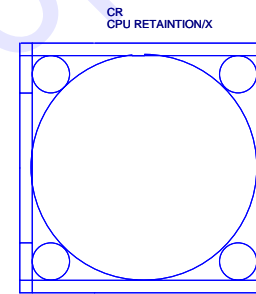
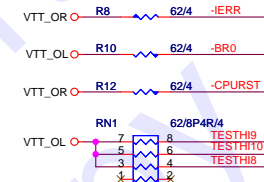
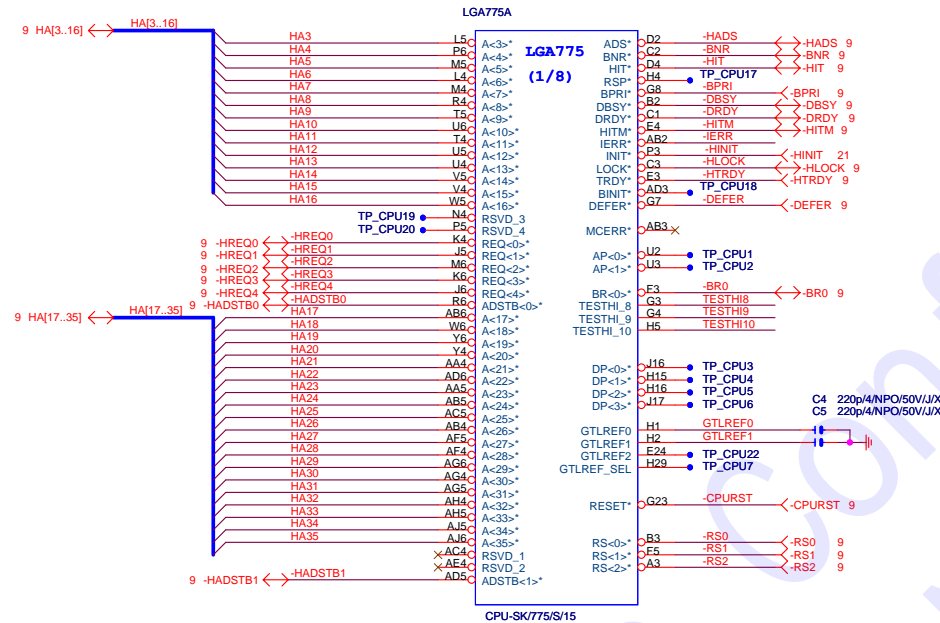
PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0	MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1	MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#	MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3	MAIN	IN	ICH_FAN_TACH3	P/U 8.2K VCC3
GP8	STBY	IN	GPIO8 (DUALBIOS_INPUT)	P/U 8.2K 3VDUAL
GP9	STBY	OUT	WOL_ONLY	P/D 100K GND
GP10	STBY	IN	CLGPIO1	P/U 8.2K 3VDUAL
GP11/SMBALERT#	STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12	STBY	IN	MB_ID0	P/U 8.2K 3VDUAL
GP13	STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14	STBY	IN	CLGPIO2	P/U 8.2K 3VDUAL
GP15	STBY	OUT	LAN_DISABLE (STP_PCI-)	N/A
GP16	MAIN	OUT/LOW	RESET	N/A
GP17/TACH0	MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18	MAIN	OUT	MB_ID1	P/U 8.2K VCC3
GP19	MAIN	IN	SATA1GP	P/U 8.2K VCC3
GP20	MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21	MAIN	IN	SATA0GP	P/U 8.2K VCC3
GP22	MAIN	IN	SCLOCK	P/U 8.2K VCC3
GP23	MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	OUT	CLGPIO0	P/U 8.2K 3VDUAL
GP25	STBY	IN	MB_ID2 (STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#	STBY	OUT	S4_STATE#	P/U 8.2K 3VDUAL
GP27	STBY	OUT/LOW	GPIO27 (EL_STATE0)	P/U 8.2K 3VDUAL
GP28	STBY	OUT/LOW	PWR_LED (EL_STATE1)	N/A
GP29/OC5#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP30/OC6#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP31/OC7#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP32	MAIN	OUT	DUAL_BIOS	P/U 100K+1M VCC3
GP33	MAIN	OUT	DUAL_BIOS	P/U 8.2K VCC3
GP34	MAIN	OUT/LOW	GPIO34/SMB_RST	N/A
GP35	MAIN	OUT	SATACLKREQ#	N/A
GP36	MAIN	IN	SATA2GP	P/U 8.2K VCC3
GP37	MAIN	IN	SATA3GP	P/U 8.2K VCC3
GP38	MAIN	IN	SLOAD	P/U 8.2K VCC3
GP39	MAIN	IN	GPIO39	P/D 8.2K GND
GP48	MAIN	IN	GPIO48	P/U 8.2K VCC3
GP49	MAIN	IN	CPUPWROK	P/U 100 VTT_OL

VCORE:3 PHASE PWM--ISL6312



Gigabyte Technology			
Title		TABLE LIST	
Size B	Document Number	P35-S3	Rev 1.02
Date:	Wednesday, August 15, 2007	Sheet 4	of 35

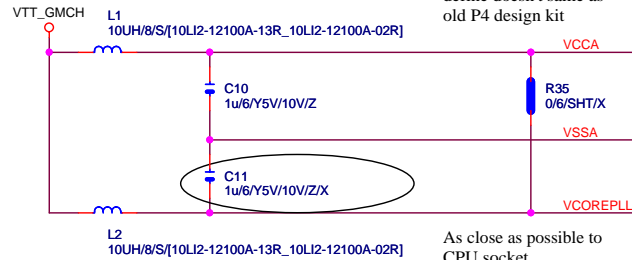
ADSTB:4/14 50+-15%



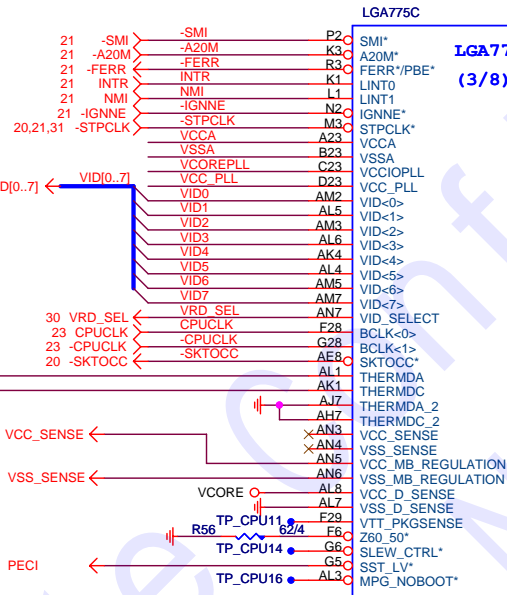
GTLREF_UV0	GTLREF_UV1	Ratio Set
HIGH	HIGH	0.67
LOW	HIGH	0.65
HIGH	LOW	0.63
LOW	LOW	0.615

Note:

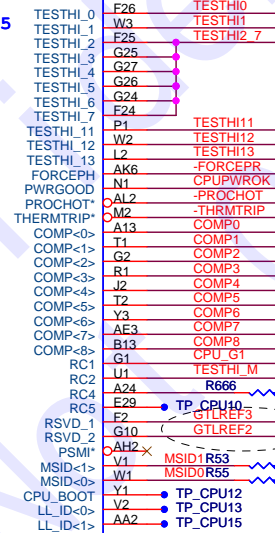
VCCA & VCOREPLL
define doesn't same as
old P4 design kit



As close as possible to
CPU socket



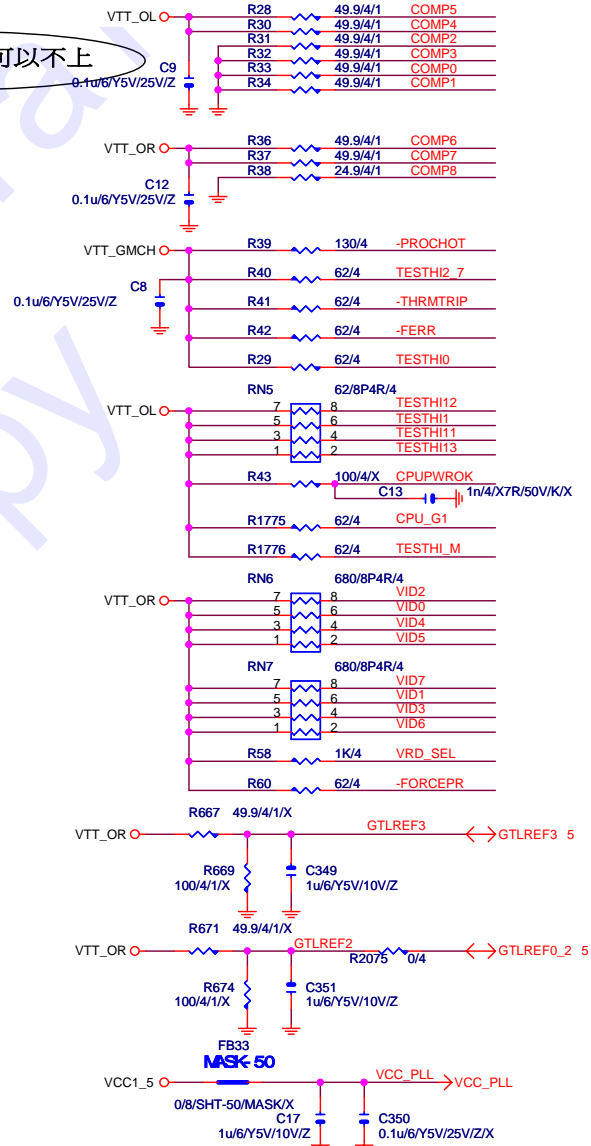
LGA775C

**LGA775
(3/8)**


CPU-SK/775/S/15

PECI:Platform Environment Control Interface

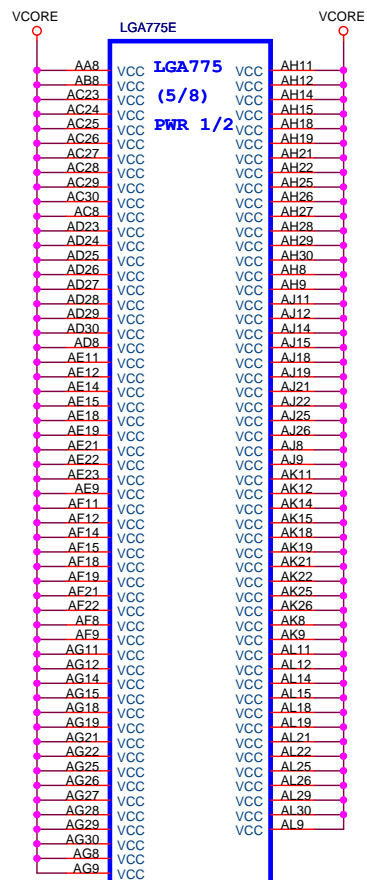
Place outside of CPU socket



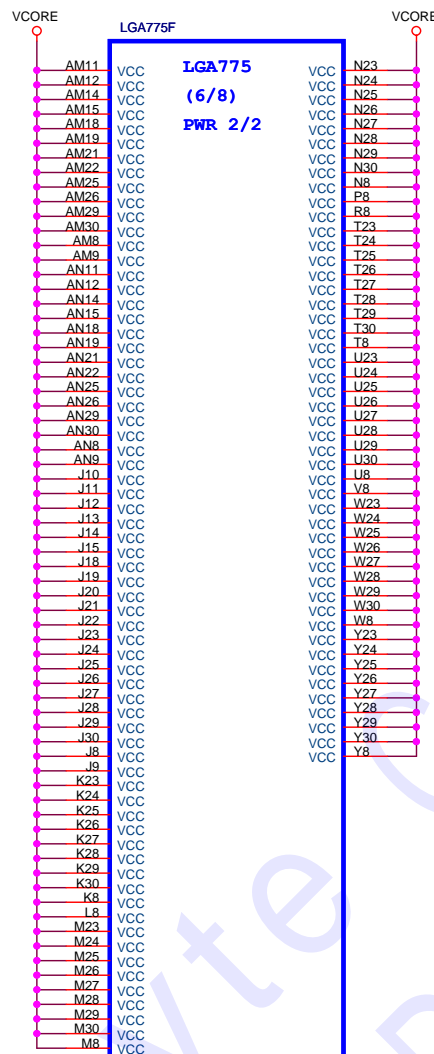
COMP4~7 可以不上

Gigabyte Technology

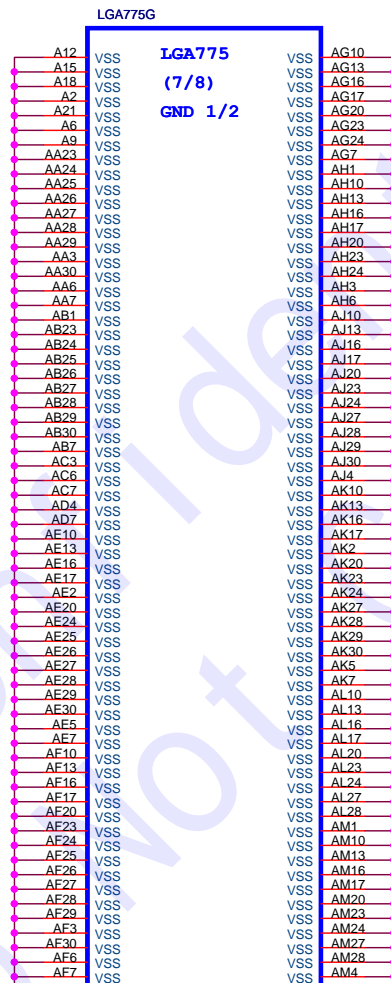
Title			P4_LGA775-C	
Size	Document Number	P35-S3		Rev
B				1.02
Date:	Wednesday, August 15, 2007	Sheet	7	of 35



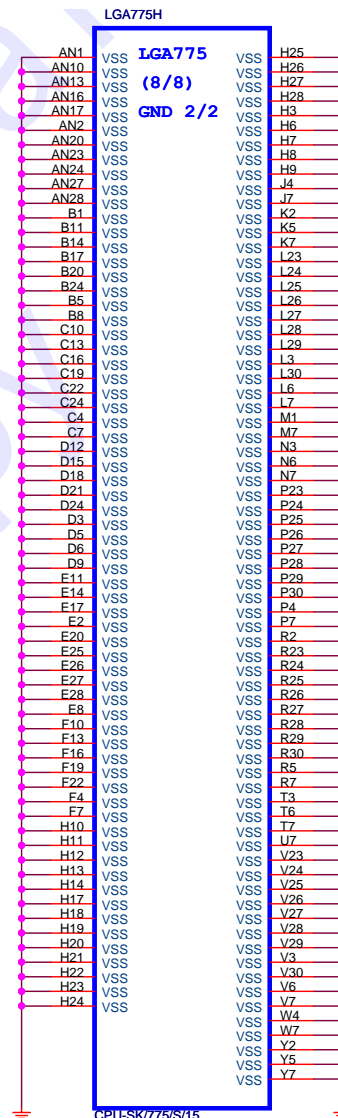
CPU-SK/775/S/15



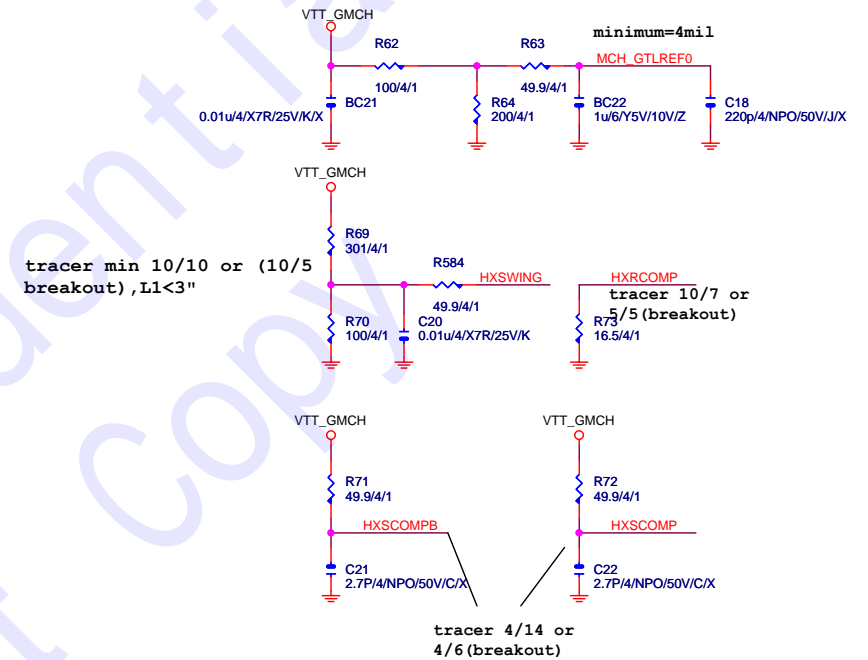
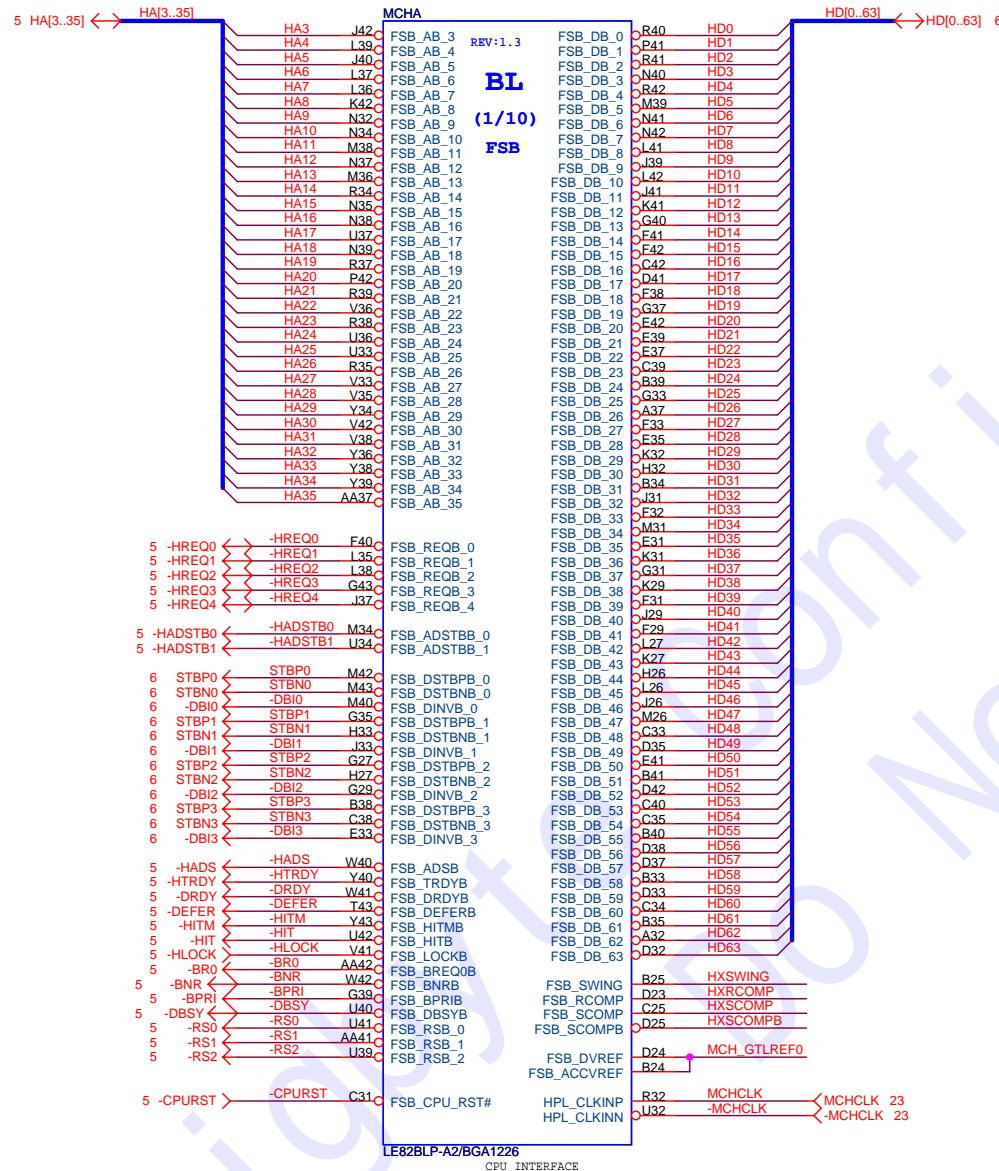
CPU-SK/775/S/15



CPU-SK/775/S/15

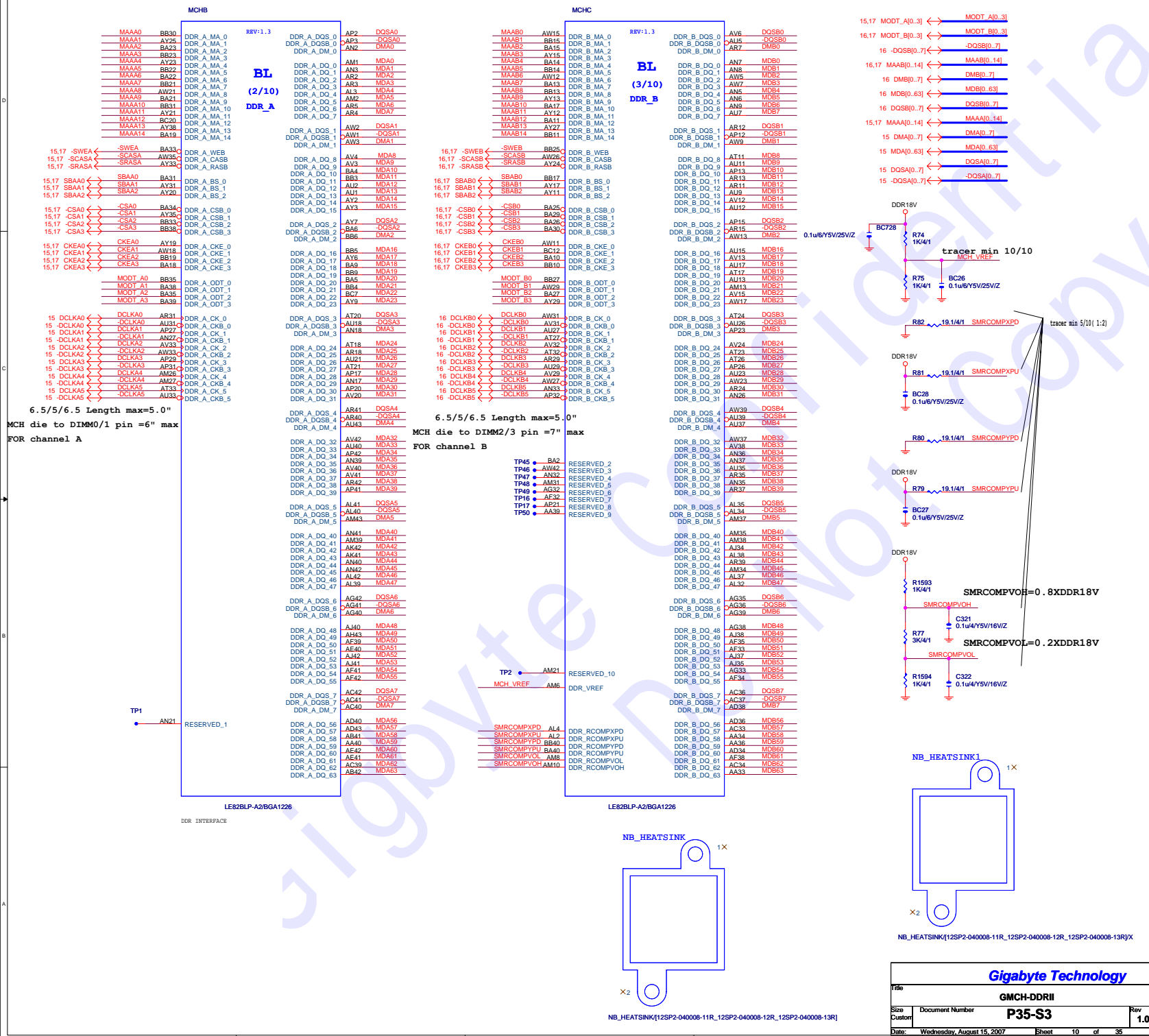


CPU-SK/775/S/15

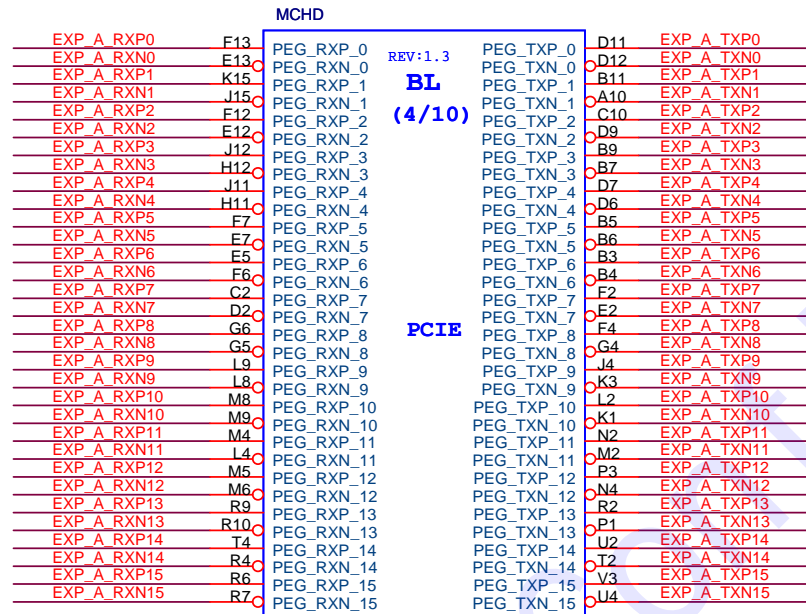


Gigabyte Technology

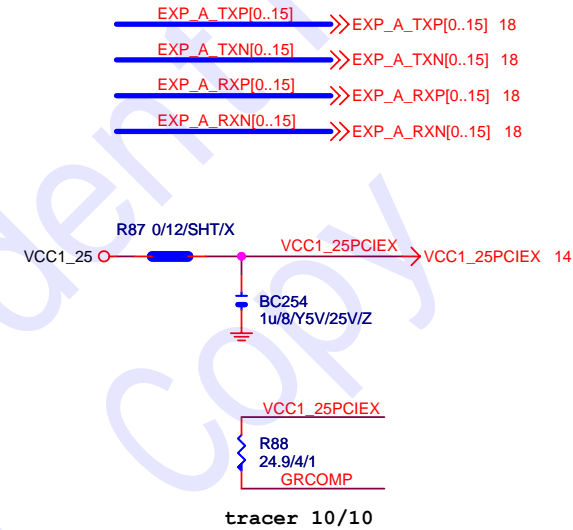
Title			
GMCH-HOST			
Size	Document Number	P35-S3	
Custom			Rev 1.02
Date:	Wednesday, August 15, 2007	Sheet	9 of 35



PCIEX16:15/4/8/4/15
Impedance=95 +- 17.5%

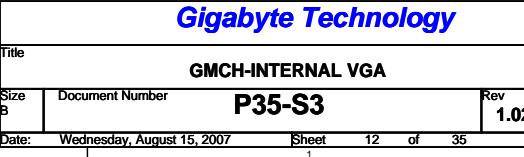


DMI:12/4/8/4/12
Impedance=95 +- 17.5%



Gigabyte Technology

Title		
GMCH-PCI E & DMI		
Size Custom	Document Number P35-S3	Rev 1.02
Date: Wednesday, August 15, 2007		
Sheet 11 of 35		



MCHG

BC37	VSS_1	REV:1.3	VSS_181	AE24
BC32	VSS_2		VSS_182	AE22
BC28	VSS_3		VSS_183	AE20
BC24	VSS_3		VSS_183	AE4
BC10	VSS_4		VSS_184	AE3
BC5	VSS_5		VSS_185	AE2
BB7	VSS_6		VSS_186	AD42
AY41	VSS_7		VSS_187	AD39
AY4	VSS_8		VSS_188	AD37
AW43	VSS_9		VSS_189	AD35
AW41	VSS_10		VSS_190	AD33
AV37	VSS_11		VSS_191	AD25
AV36	VSS_12		VSS_192	AD23
AV27	VSS_13		VSS_193	AD21
AV23	VSS_14		VSS_194	AD19
AV21	VSS_15		VSS_195	AC38
AV17	VSS_16		VSS_196	AC35
AV11	VSS_17		VSS_197	AC24
AV9	VSS_18		VSS_198	AC22
AV7	VSS_19		VSS_199	AC20
AV2	VSS_20		VSS_200	AC10
AU42	VSS_21		VSS_201	AC7
AU38	VSS_22		VSS_202	AC5
AU32	VSS_23		VSS_203	AB43
AU24	VSS_24		VSS_204	AB25
AU20	VSS_25		VSS_205	AB23
AU6	VSS_26		VSS_206	AB21
AU4	VSS_27		VSS_207	AB19
AT31	VSS_28		VSS_208	AB2
AT29	VSS_29		VSS_209	AB1
AT15	VSS_30		VSS_210	AA38
AT13	VSS_31		VSS_211	AA35
AT12	VSS_32		VSS_212	AA24
AR38	VSS_33		VSS_213	AA22
AR33	VSS_34		VSS_214	AA20
AR32	VSS_35		VSS_215	AA8
AR27	VSS_36		VSS_216	AA5
AR26	VSS_37		VSS_217	Y42
AR23	VSS_38		VSS_218	Y37
AR21	VSS_39		VSS_219	Y35
AR20	VSS_40		VSS_220	Y33
AR17	VSS_41		VSS_221	Y25
AR9	VSS_42		VSS_222	Y23
AR6	VSS_43		VSS_223	Y21
AP43	VSS_44		VSS_224	Y19
AP24	VSS_45		VSS_225	Y10
AP18	VSS_46		VSS_226	Y7
AP1	VSS_47		VSS_227	Y5
AN38	VSS_48		VSS_228	Y1
AN31	VSS_49		VSS_229	W24
AN29	VSS_50		VSS_230	W22
AN24	VSS_51		VSS_231	W20
AN23	VSS_52		VSS_232	W3
AN20	VSS_53		VSS_233	W43
AN13	VSS_54		VSS_234	V39
AN12	VSS_55		VSS_235	V37
AN11	VSS_56		VSS_236	V34
AN4	VSS_57		VSS_237	V32
AM42	VSS_58		VSS_238	V11
AM40	VSS_59		VSS_239	V8
AM36	VSS_60		VSS_240	V5
AM33	VSS_61		VSS_241	V2
AM29	VSS_62		VSS_242	U38
AM24	VSS_63		VSS_243	U35
AM23	VSS_64		VSS_244	U8
AM20	VSS_65		VSS_245	U7
AM11	VSS_66		VSS_246	U5
AM9	VSS_67		VSS_247	T42
AM7	VSS_68		VSS_248	T1
AM4	VSS_69		VSS_249	R36
AL36	VSS_70		VSS_250	R33
AL33	VSS_71		VSS_251	R31
AL31	VSS_72		VSS_252	R11
AK43	VSS_73		VSS_253	R8
AJ39	VSS_74		VSS_254	R5
AJ36	VSS_75		VSS_255	R3
AJ33	VSS_76		VSS_256	P43
AJ32	VSS_77		VSS_257	P30
AH42	VSS_78		VSS_258	P21
AG37	VSS_79		VSS_259	P18
AG34	VSS_80		VSS_260	P17
AF43	VSS_81		VSS_261	P2
AF37	VSS_82		VSS_262	N36
AF36	VSS_83		VSS_263	N33
AF10	VSS_84		VSS_264	N31
AF9	VSS_85		VSS_265	N27
AF8	VSS_86		VSS_266	N21
AF7	VSS_87		VSS_267	N13
AF6	VSS_88		VSS_268	N10
AF5	VSS_89		VSS_269	N7
	VSS_90		VSS_270	

LE82BLP-A2/BGA1226

MCHG

N5	VSS_91	REV:1.3	VSS_271	B10
M37	VSS_92		VSS_272	A39
M35	VSS_93		VSS_273	A34
M33	VSS_94		VSS_274	A26
M27	VSS_95		VSS_275	A18
M21	VSS_96		VSS_276	A12
M20	VSS_97		VSS_277	A7
M17	VSS_98		VSS_278	BC41
M15	VSS_99		VSS_279	BC3
M10	VSS_100		VSS_280	BA1
M7	VSS_101		VSS_281	AY40
M1	VSS_102		VSS_282	AF23
L40	VSS_103		VSS_283	AF21
L33	VSS_104		VSS_284	AF19
L32	VSS_105		VSS_285	AE18
L31	VSS_106		VSS_286	AC18
L29	VSS_107		VSS_287	AA18
L21	VSS_108		VSS_288	V29
L20	VSS_109		VSS_289	U29
L11	VSS_110		VSS_290	U27
L7	VSS_111		VSS_291	R21
L5	VSS_112		VSS_292	E1
L3	VSS_113		VSS_293	C43
K43	VSS_114		VSS_294	C1
K26	VSS_115		VSS_295	A41
K21	VSS_116		VSS_296	A5
K18	VSS_117		VSS_297	A3
K13	VSS_118		VSS_298	V30
K12	VSS_119		VSS_299	
K2	VSS_120		VSS_300	
J38	VSS_121		VSS_301	
J35	VSS_122		VSS_302	
J32	VSS_123		VSS_303	
J27	VSS_124		VSS_304	
J21	VSS_125		VSS_305	
J9	VSS_126		VSS_306	
J7	VSS_127		VSS_307	
J5	VSS_128		VSS_308	
H31	VSS_129		VSS_309	
H29	VSS_130		VSS_310	
H21	VSS_131		VSS_311	
H20	VSS_132		VSS_312	
H17	VSS_133		VSS_313	
H15	VSS_134		VSS_314	
H13	VSS_135		VSS_315	
G42	VSS_136		VSS_316	
G38	VSS_137		VSS_317	
G32	VSS_138		VSS_318	
G21	VSS_139		VSS_319	
G13	VSS_140		VSS_320	
G12	VSS_141		VSS_321	
G11	VSS_142		VSS_322	
G9	VSS_143		VSS_323	
G7	VSS_144		VSS_324	
G1	VSS_145		VSS_325	
F37	VSS_146		VSS_326	
F35	VSS_147		VSS_327	
F27	VSS_148		VSS_328	
F21	VSS_149		VSS_329	
F18	VSS_150		VSS_330	
F15	VSS_151		VSS_331	
F3	VSS_152		VSS_332	
E43	VSS_153		VSS_333	
E32	VSS_154		VSS_334	
E24	VSS_155		VSS_335	
E21	VSS_156		VSS_336	
E11	VSS_157		VSS_337	
E9	VSS_158		VSS_338	
E3	VSS_159		VSS_339	
D40	VSS_160		VSS_340	
D31	VSS_161		VSS_341	
D21	VSS_162		VSS_342	
D17	VSS_163		VSS_343	
D15	VSS_164		VSS_344	
D3	VSS_165		VSS_345	
C26	VSS_166		VSS_346	
C11	VSS_167		VSS_347	
C6	VSS_168		VSS_348	
C5	VSS_169		VSS_349	
C4	VSS_170		VSS_350	
B37	VSS_171		VSS_351	
B32	VSS_172		VSS_352	
B31	VSS_173		VSS_353	
B26	VSS_174		VSS_354	
B23	VSS_175		VSS_355	
B22	VSS_176		VSS_356	
B19	VSS_177		VSS_357	
B14	VSS_178		VSS_358	
	VSS_179		VSS_359	
D16	VSS_180		VSS_360	
M11	VSS_181		VSS_361	

LE82BLP-A2/BGA1226

Gigabyte Technology

Title

GMCH-GND

Size
Custom

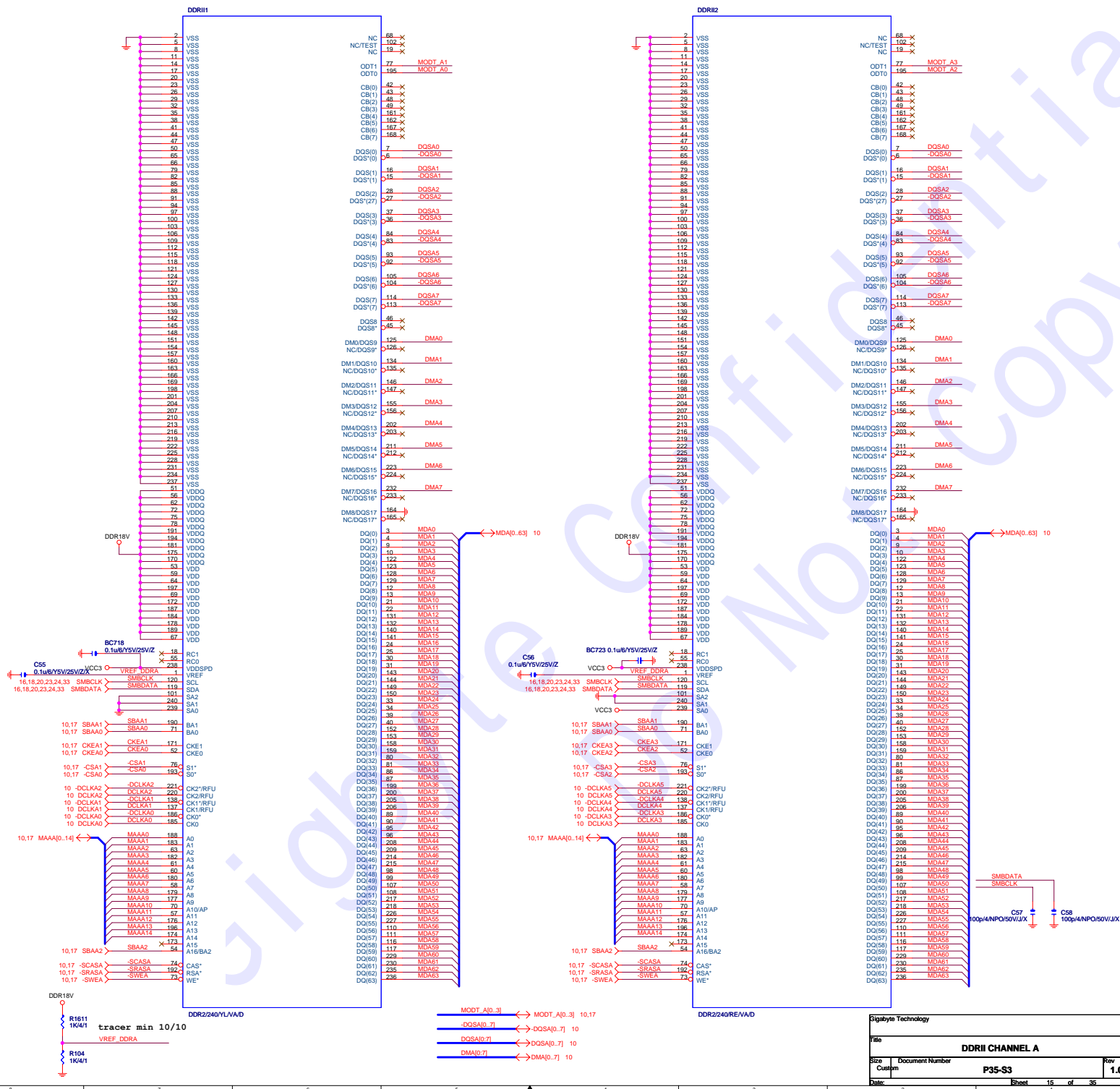
Document Number

P35-S3

Rev
1.02

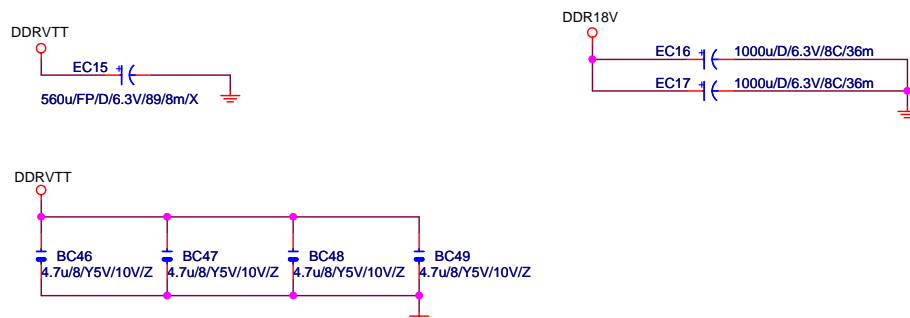
Date: Wednesday, August 15, 2007

Sheet 13 of 35



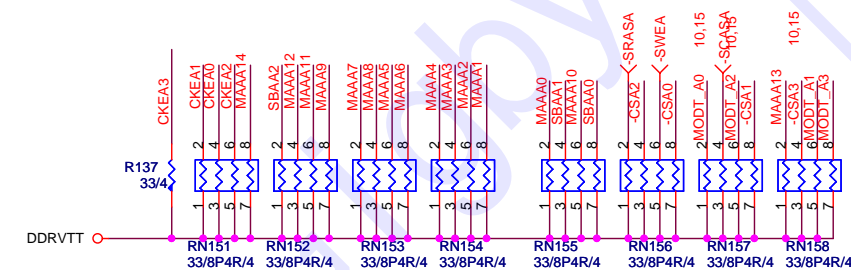
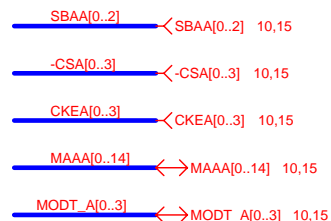
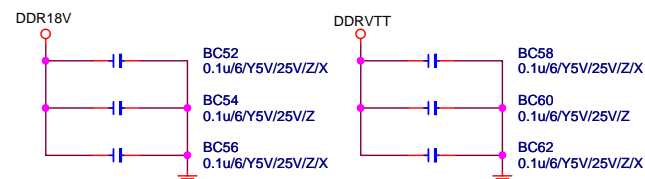
DDR TERMINATION CHANNEL A

DDRVTT Decouple



DDR18V Decouple

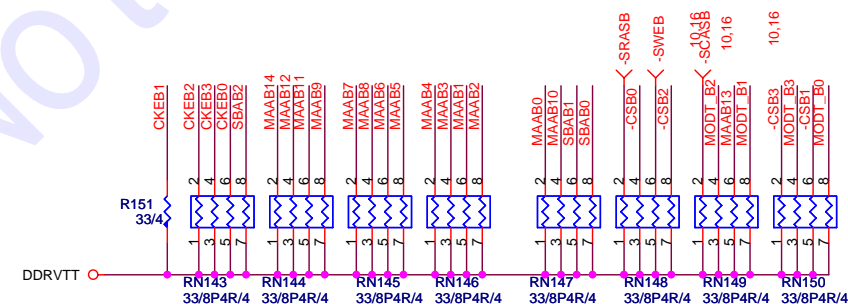
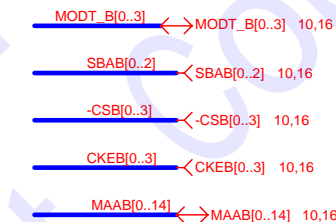
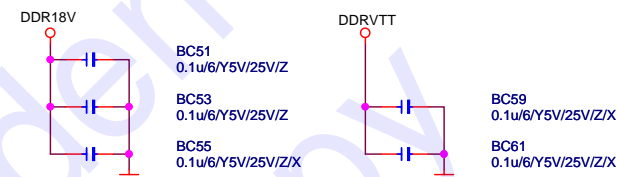
DDRVTT Decouple

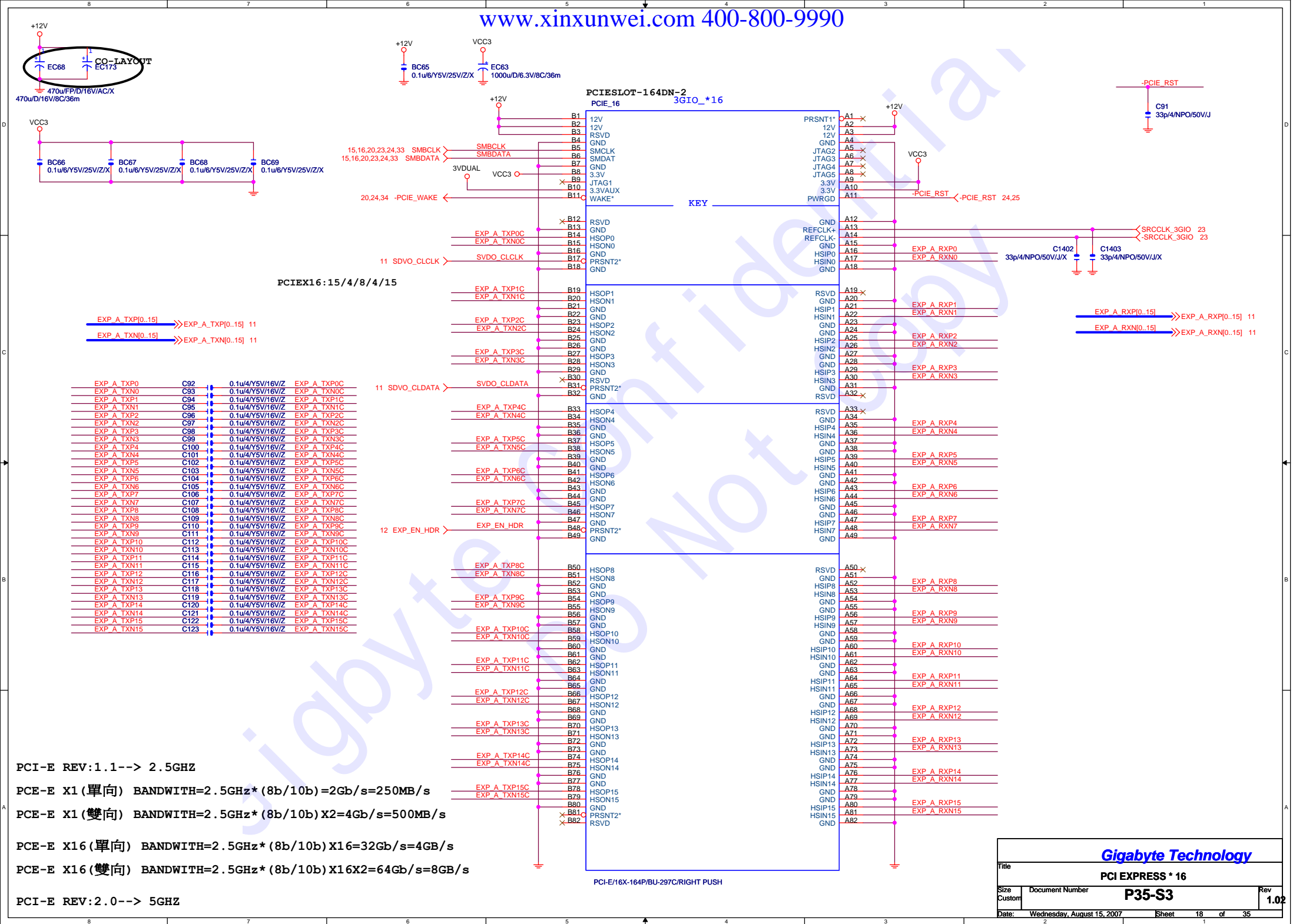


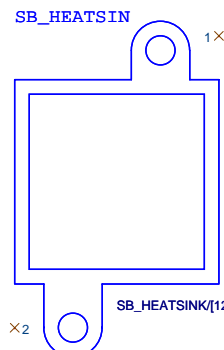
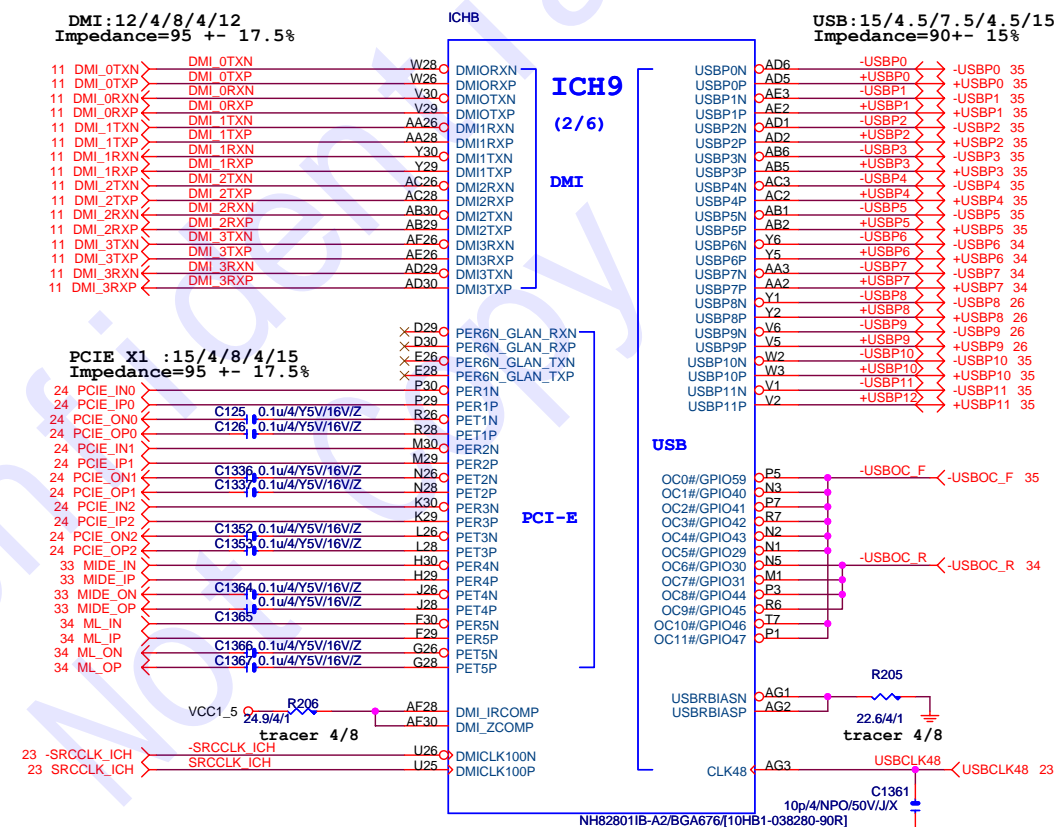
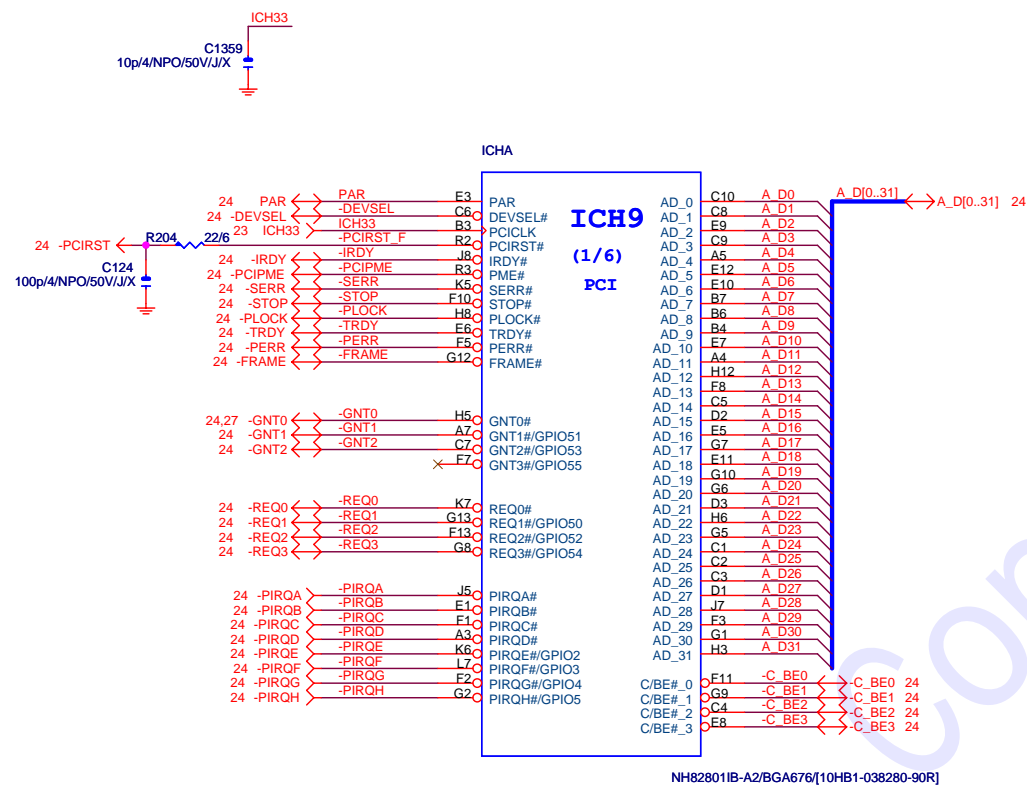
DDR TERMINATION CHANNEL B

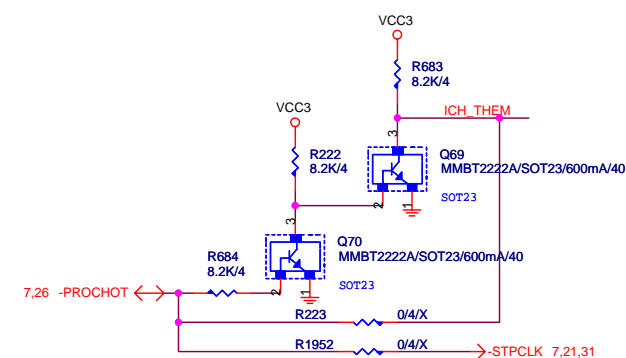
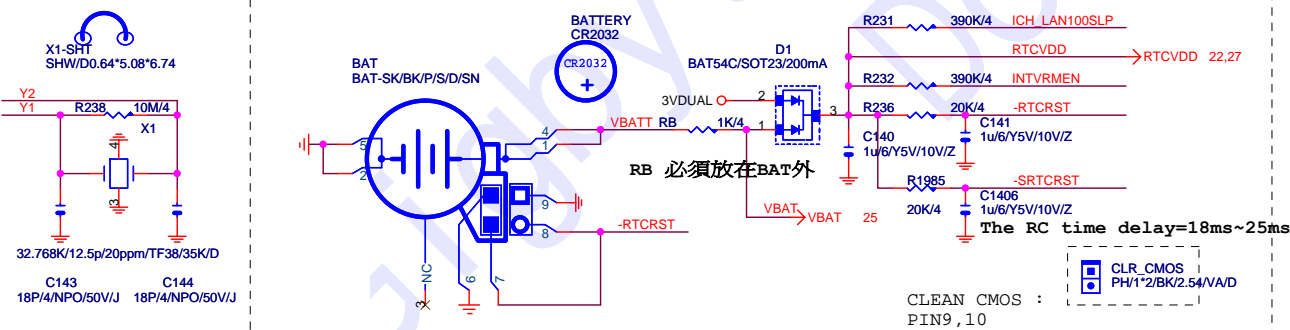
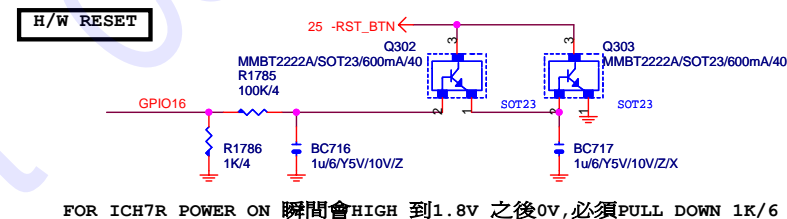
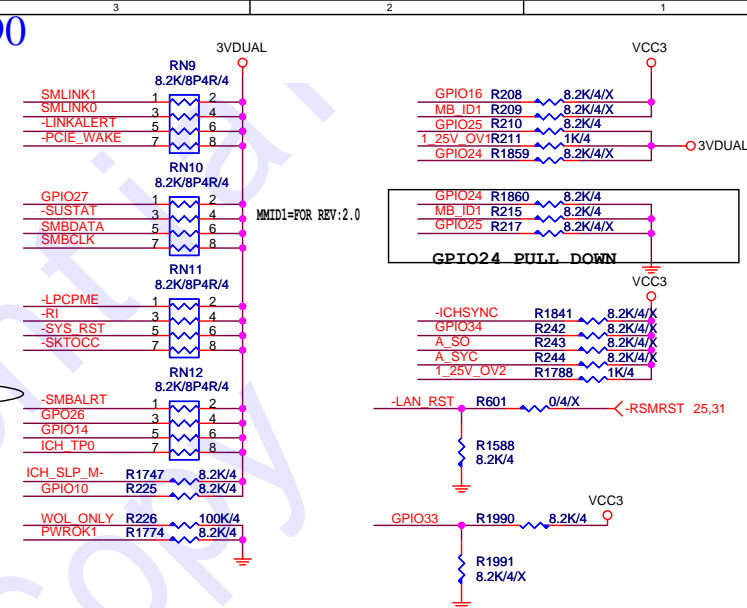
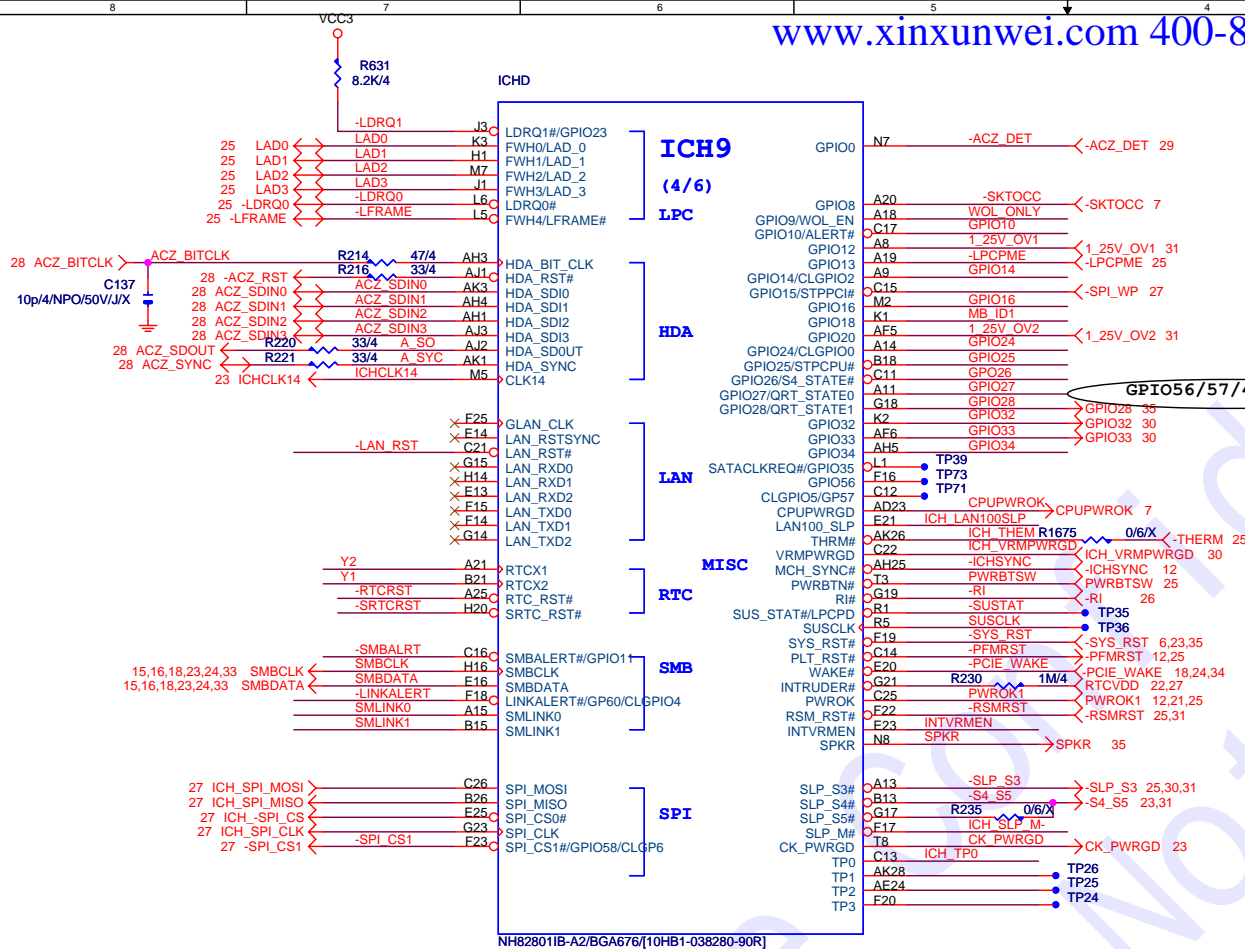
DDR18V Decouple

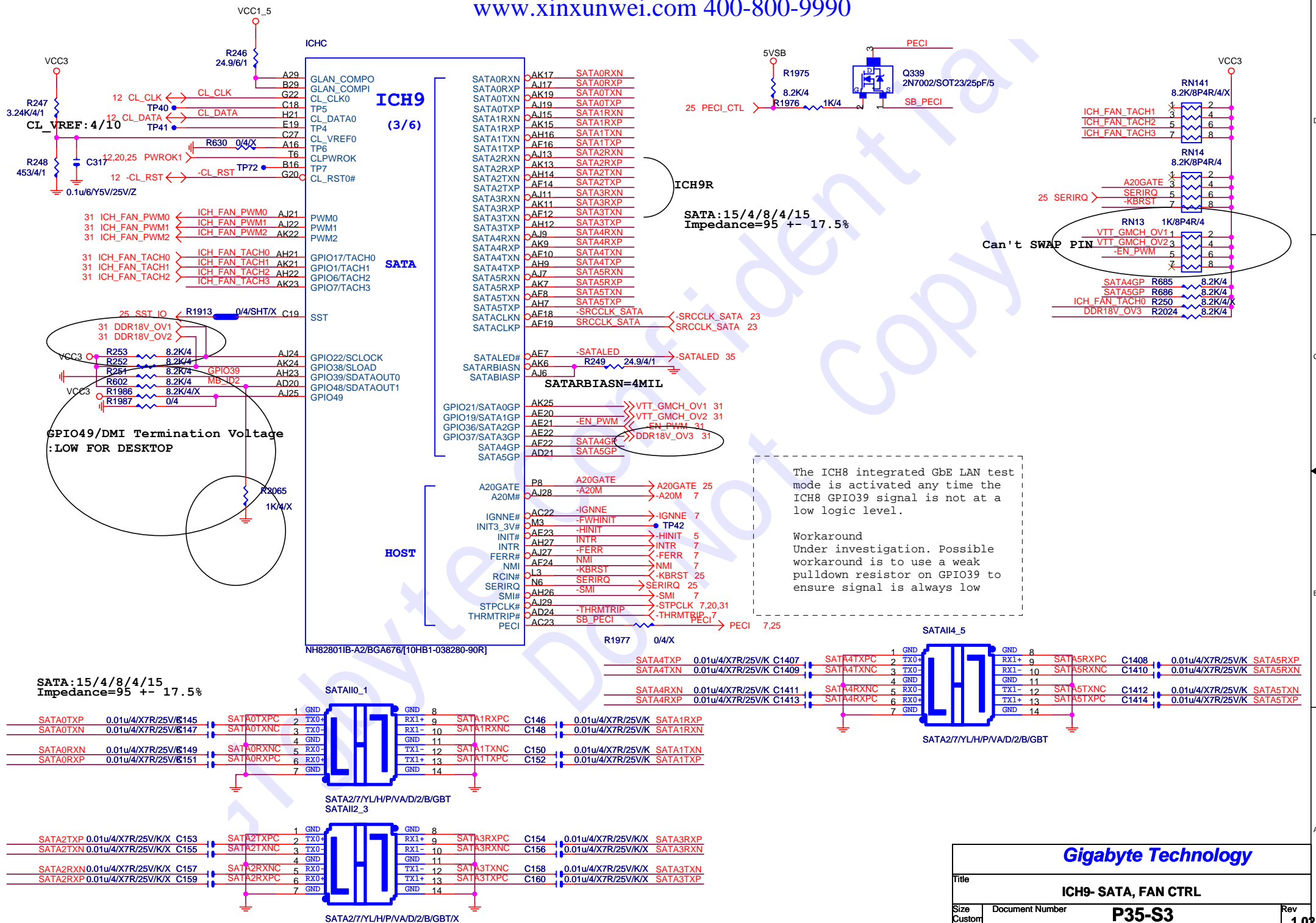
DDRVTT Decouple











CLK GEN CK505

50歐姆: [18/4/10/4/18]

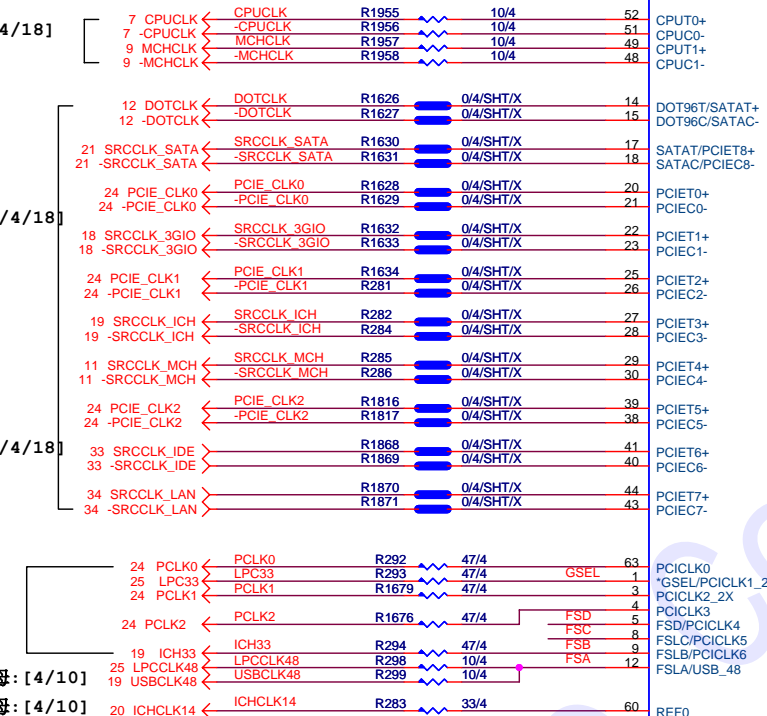
50歐姆: [18/4/10/4/18]

50歐姆: [18/4/10/4/18]

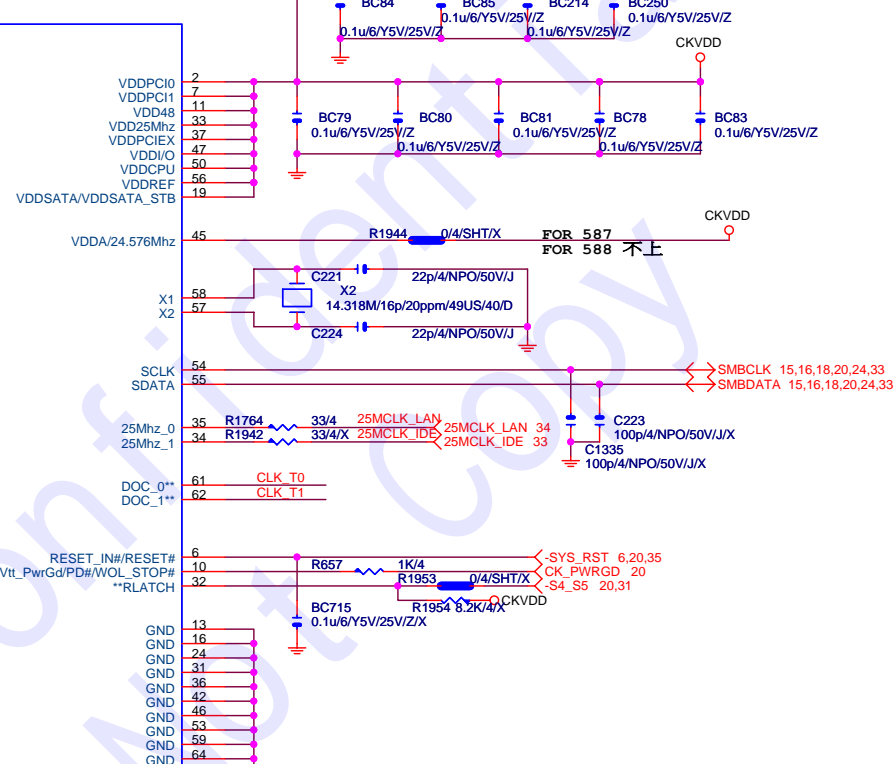
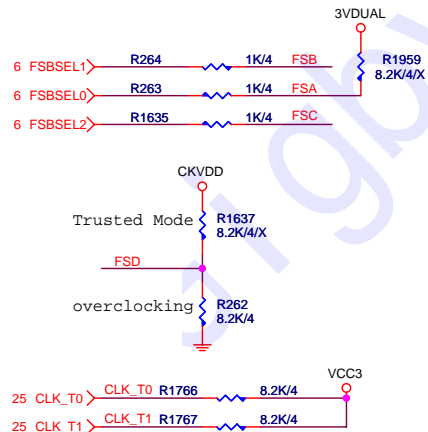
50歐姆: [4/10]

50歐姆: [4/10]

50歐姆: [4/10]



ICS9LPRS587EGLF-T/TSSOP64
 GSEL=1,96Mhz from 14/15,SATACLK from 17/18
 GSEL=0,SATACLK from 14/15,PCIECLK from 17/18



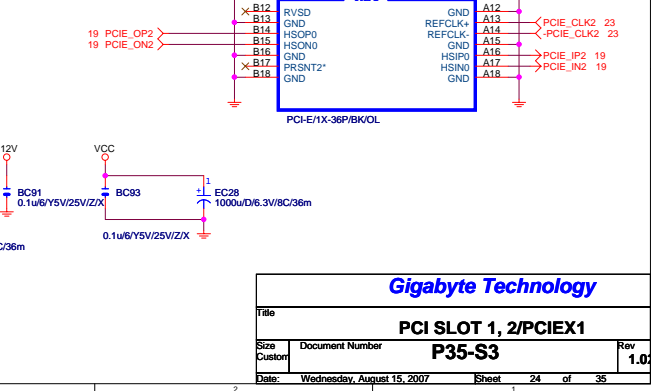
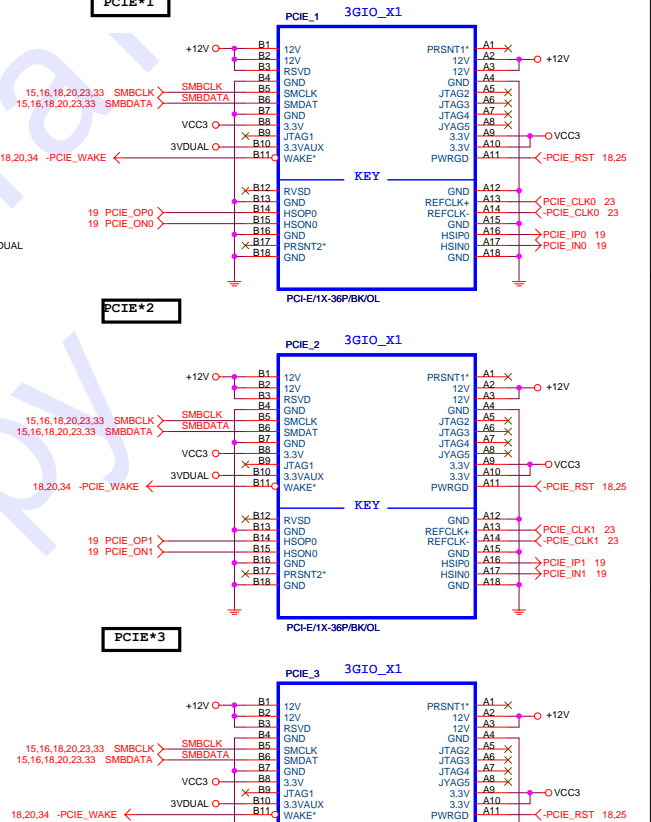
25MCLK_LAN	C1334	10p/4/NPO/50V/J/X
25MCLK_IDE	C1393	10p/4/NPO/50V/J/X
ICHCLK14	C1291	10p/4/NPO/50V/J/X
PCLK0	C214	10p/4/NPO/50V/J/X
PCLK1	C215	10p/4/NPO/50V/J/X
ICH33	C216	10p/4/NPO/50V/J/X
LPC33	C218	10p/4/NPO/50V/J/X
USBCLK48	C219	10p/4/NPO/50V/J/X
LPCCLK48	C220	10p/4/NPO/50V/J/X
PCLK2	C1298	10p/4/NPO/50V/J/X
CPUCLK	C1396	10p/4/NPO/50V/J
-CPUCLK	C1397	10p/4/NPO/50V/J
MCHCLK	C1398	10p/4/NPO/50V/J/X
-MCHCLK	C1399	10p/4/NPO/50V/J/X
SRCCLK_3GIO	C1400	10p/4/NPO/50V/J/X
-SRCCLK_3GIO	C1401	10p/4/NPO/50V/J/X

Gigabyte Technology

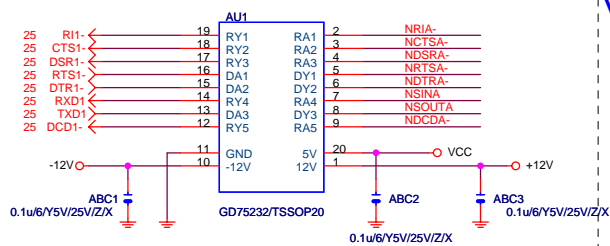
CK505 CLK GEN

P35-S3

Rev 1.02

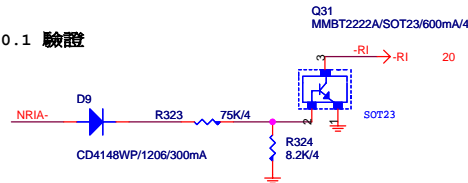


COMA

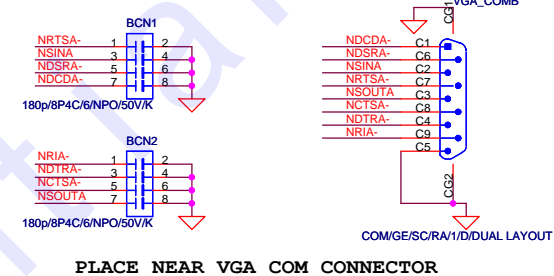


COM RI

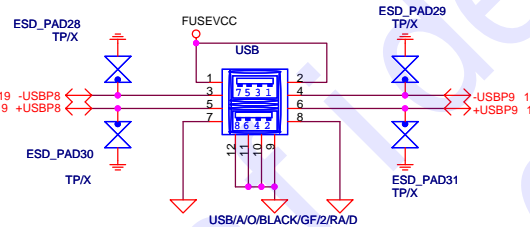
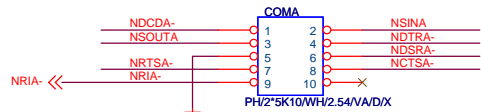
REV:0.1 驗證



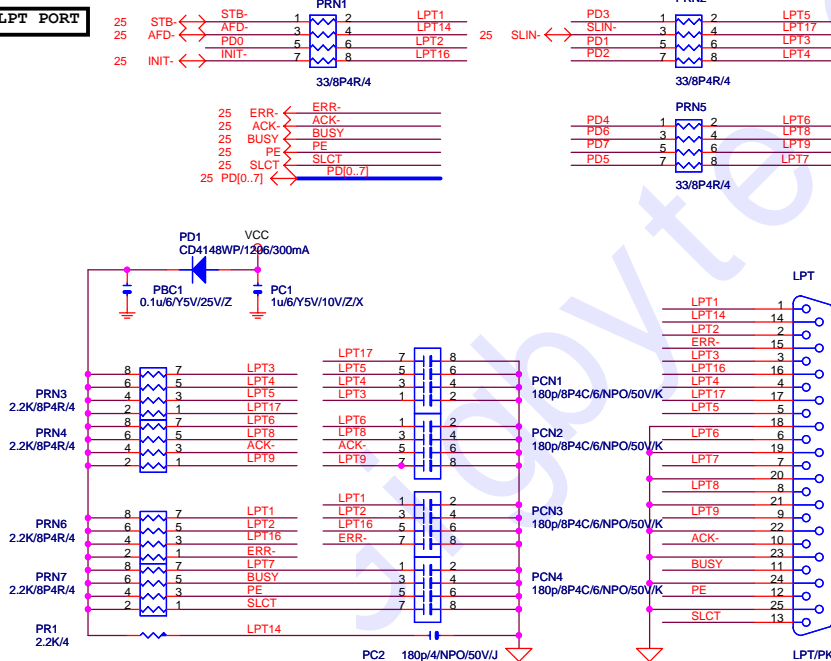
EXTERNAL COMB



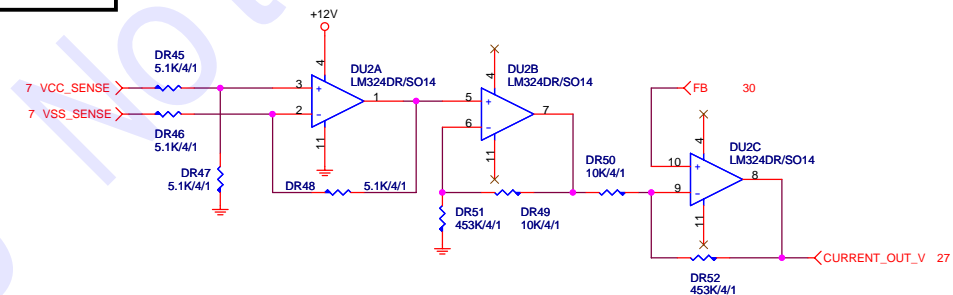
PLACE NEAR VGA_COM CONNECTOR



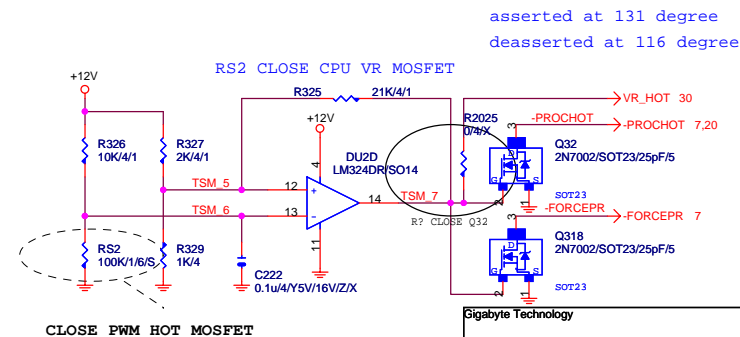
LPT PORT



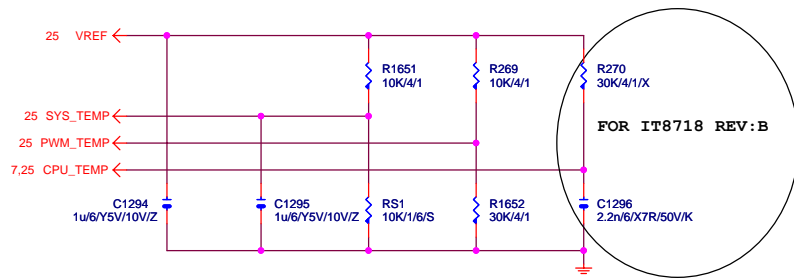
DYNAMIC CURRENT OC



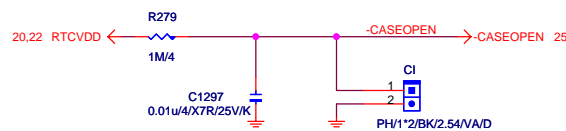
-PROHOT

asserted at 131 degree
deasserted at 116 degree

TEMP H/W MONITOR

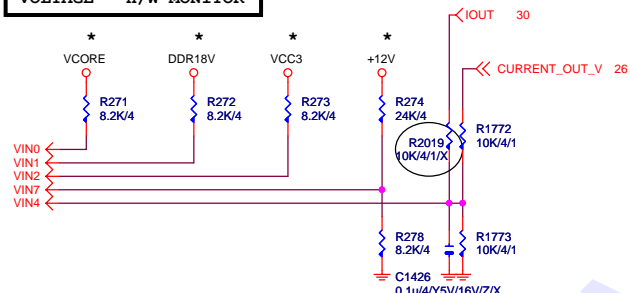


CASE OPEN

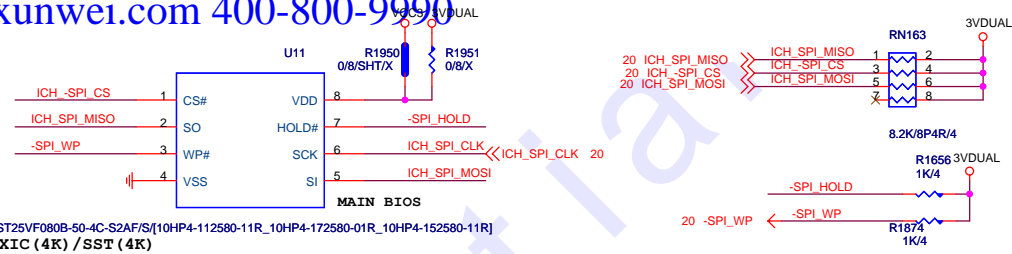
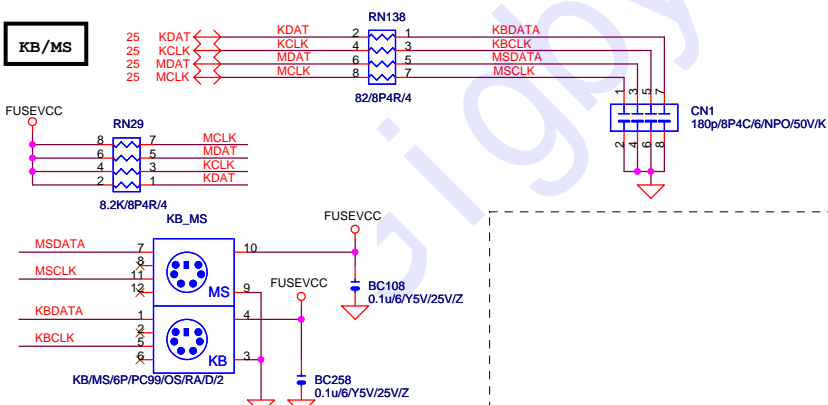


Case Open Circuits

VOLTAGE-- H/W MONITOR



KB/MS

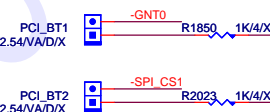


BOOT DEVICE	GNT0	CS1
SPI	0	1
PCI	1	0
F'WH	1	1

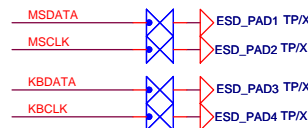
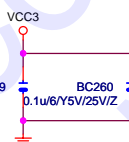
PCI_BT1



JP/1*2/BU/OH/O: [1-2]CLOSE/X



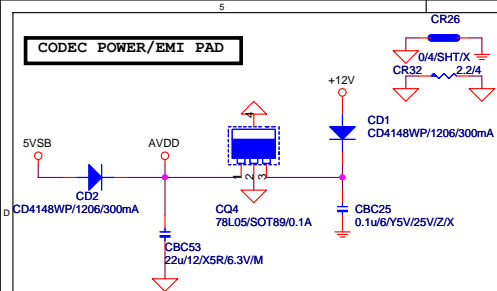
FOR DEBUG



Gigabyte Technology

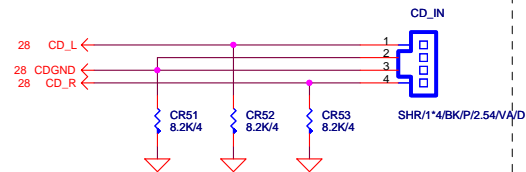
Title	BIOS/HW-MONITOR/CI/KB/MS		
Size	Document Number	P35-S3	Rev
Custom			1.02
Date:	Wednesday, August 15, 2007	Sheet	27 of 35

CODEC POWER/EMI PAD

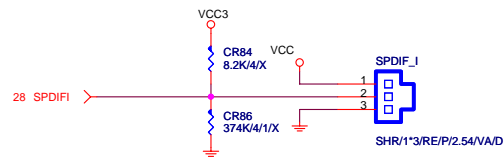


CO-LAYOUT

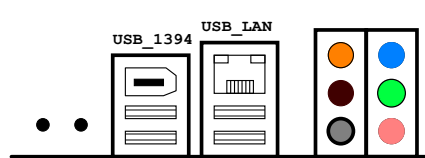
CD IN



SPDIF

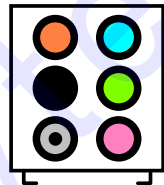


AZALIA JACK



3R2P/26P/OR, BK, GY, BU, GE, PK, RA/D/1/B
VISTA規範: REAR--->BLK, CEN/SUB--->ORG

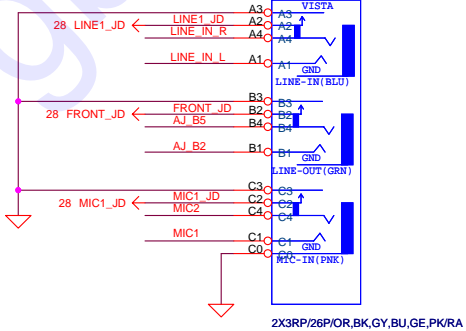
BTX AZALIA CONNECTOR



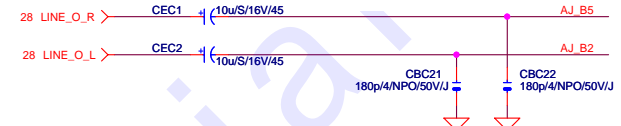
AUDIOA



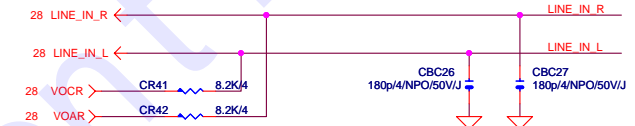
AUDIOB



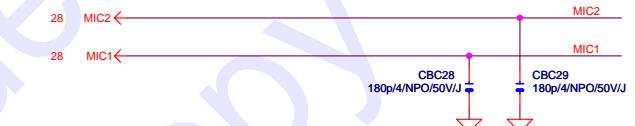
LINE-OUT



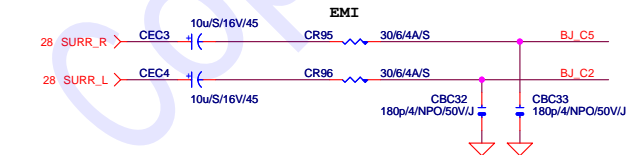
LINE-IN



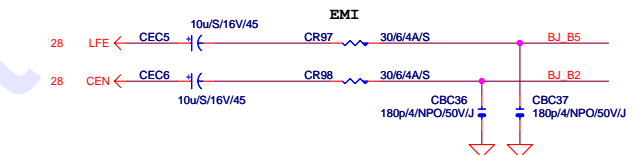
MIC-IN



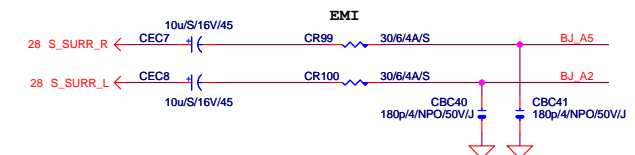
SURROUND



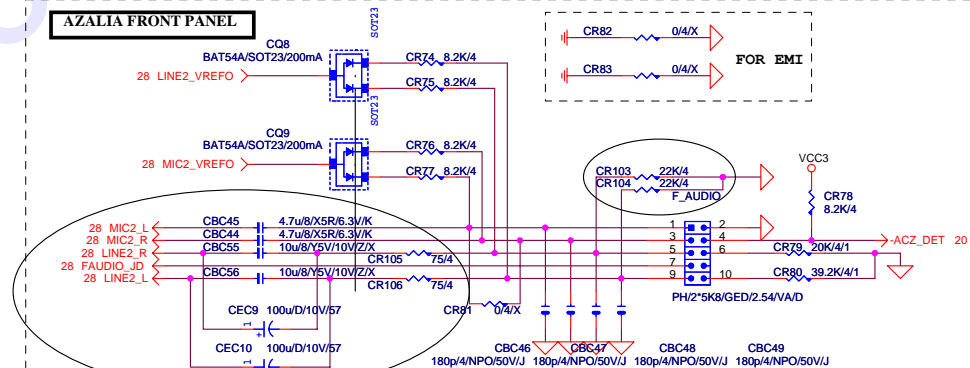
CEN/LFE



SURR BACK



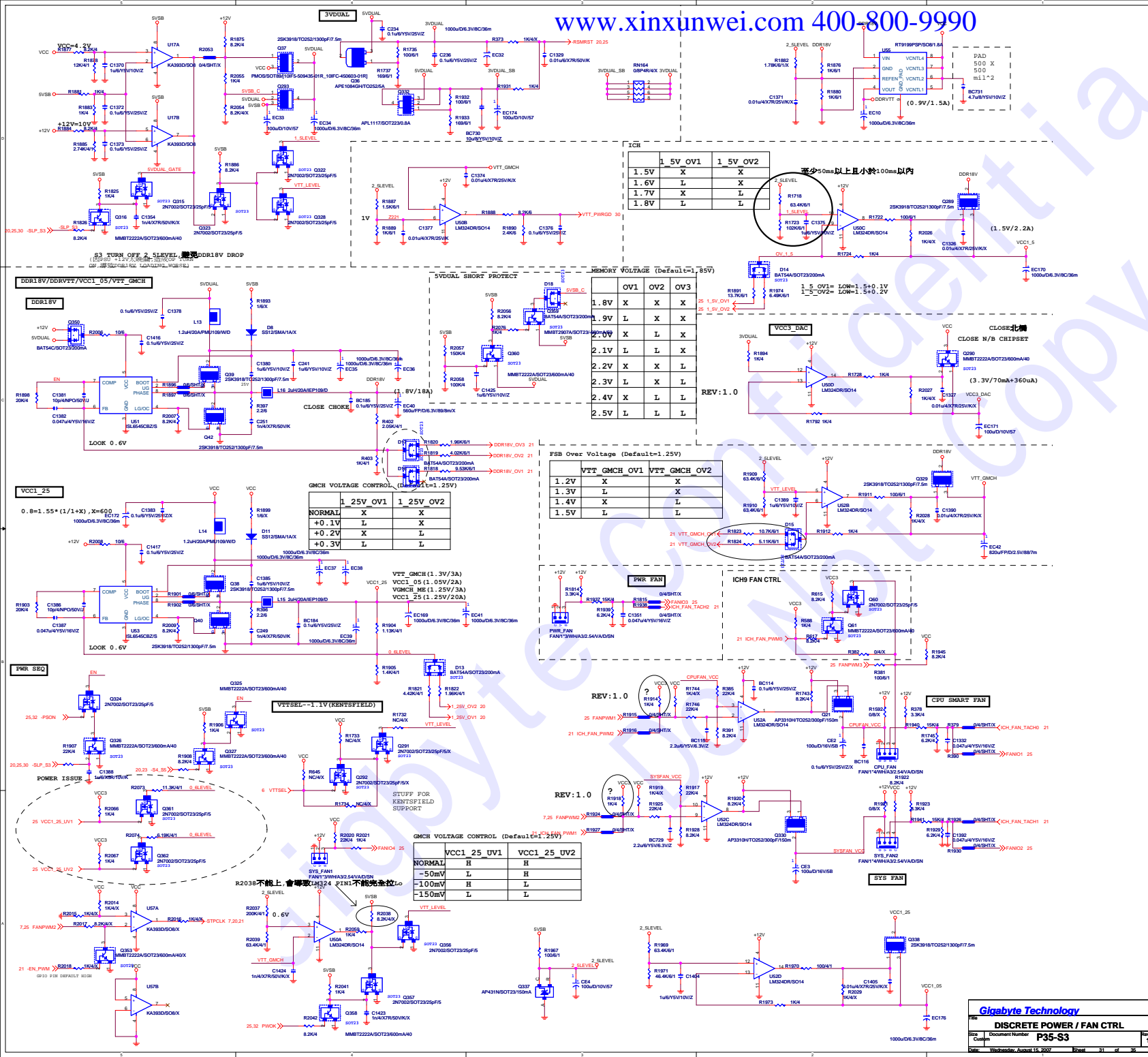
AZALIA FRONT PANEL



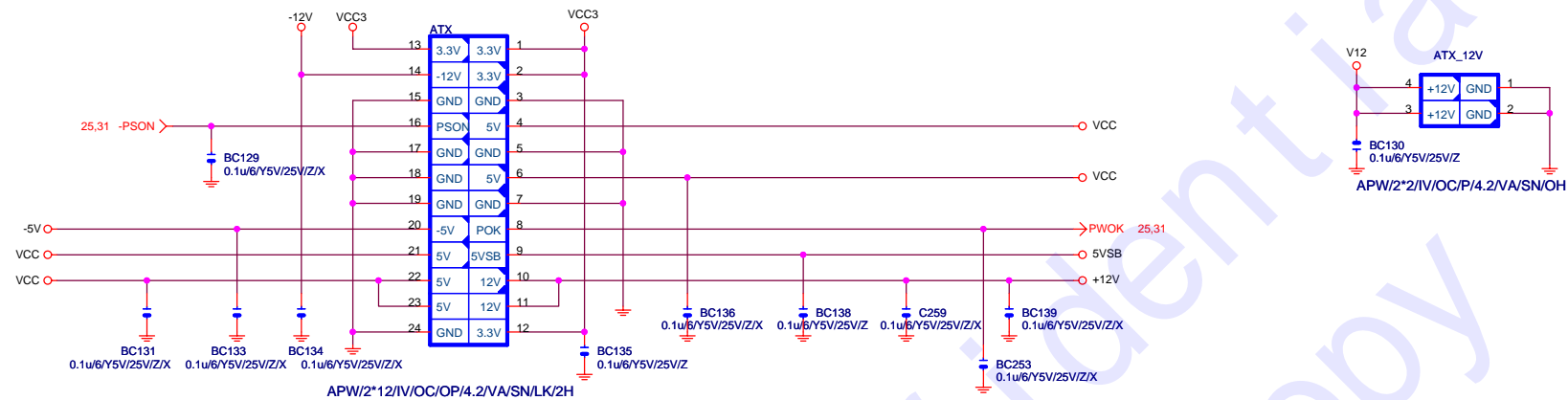
Gigabyte Technology

Title				
AUDIO JACK				
Size	Document Number			Rev
Custom	P35-S3			1.02
Date:	Wednesday, August 15, 2007		Sheet 29 of 35	

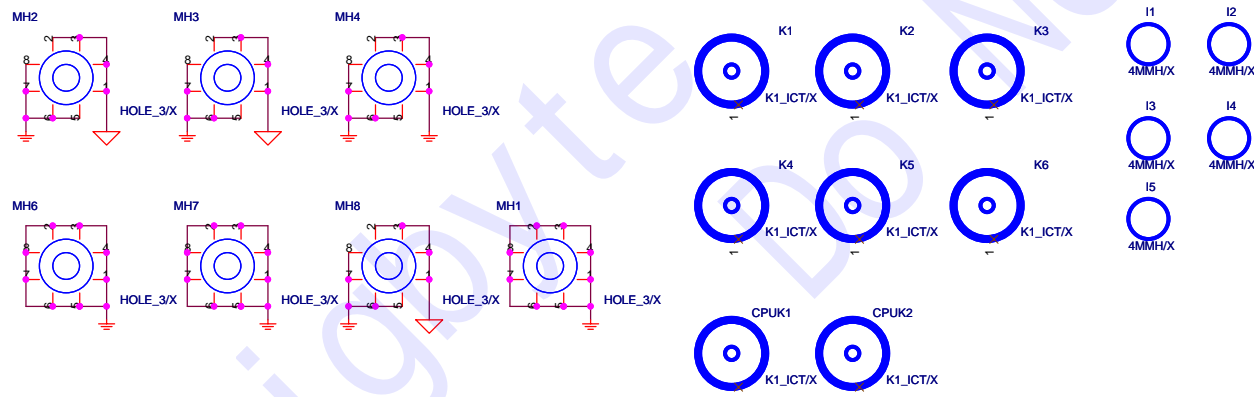




ATX POWER CONNECTOR



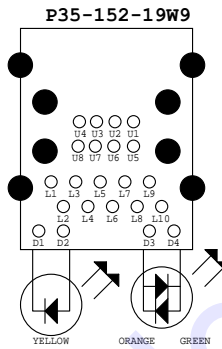
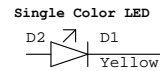
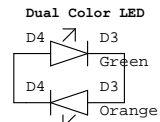
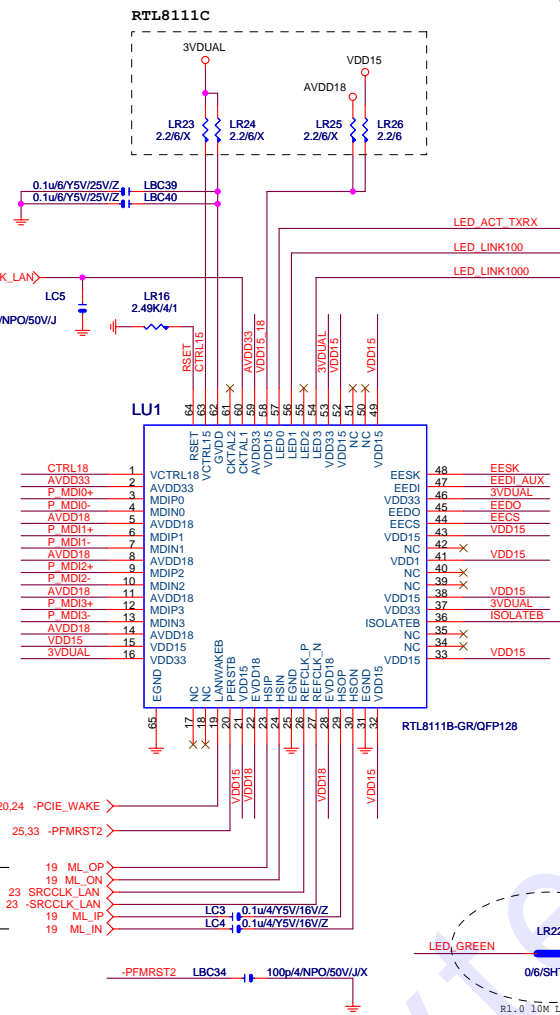
HOLE_3-2--->有鉛



Gigabyte Technology

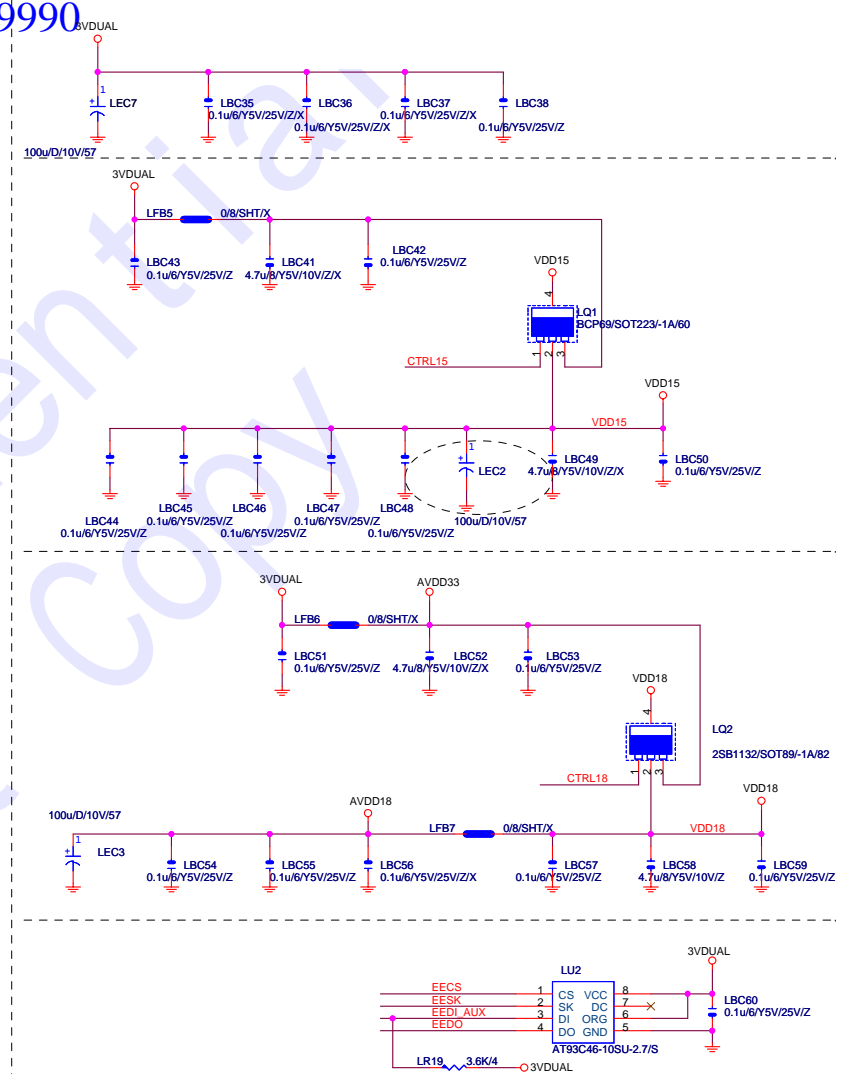
Title			
ATX POWER CONNECTOR			
Size B	Document Number	P35-S3	Rev 1.02
Date:	Wednesday, August 15, 2007	Sheet 32 of 35	

PCIE-1G LAN



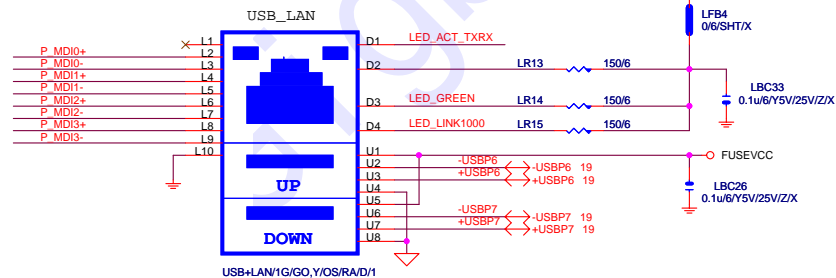
Power domain chart

	RTL8111B / RTL8101E	RTL8111C	
AVDD33	3.3V	3.3V	
AVDD18	1.8V	1.2V	
EVDD18	1.8V	1.2V	
DVDD15	1.5V	1.2V	



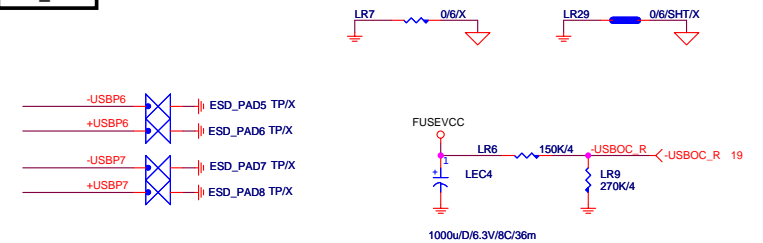
USB_LAN CONNECTOR

LAN 100 歐姆: [30/4/8/4/30] FOR B 製程



90 歐姆: [15/4.5/7.5/4.5/15]

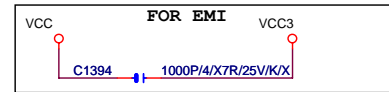
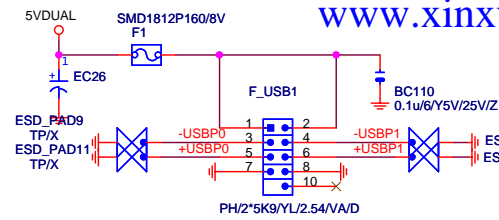
USB_LAN



FRONT USB1

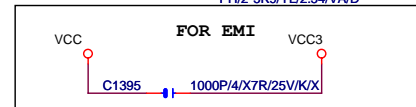
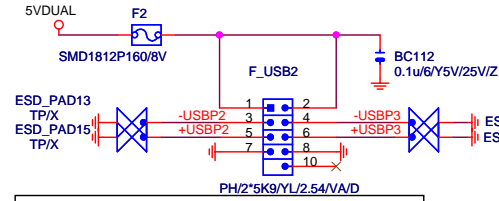
19 +USBP0 <-> +USBP0
19 -USBP0 <-> -USBP0
19 +USBP1 <-> +USBP1
19 -USBP1 <-> -USBP1

1000u/D/6.3V/8C/36m



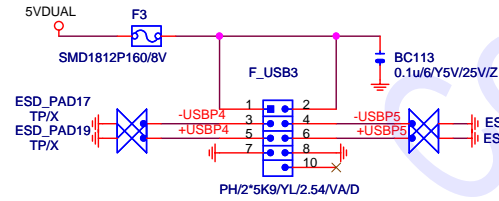
FRONT USB2

19 +USBP2 <-> +USBP2
19 -USBP2 <-> -USBP2
19 +USBP3 <-> +USBP3
19 -USBP3 <-> -USBP3



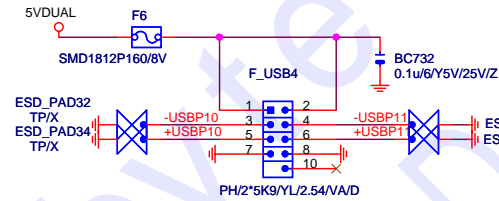
FRONT USB3

19 -USBP4 <-> -USBP4
19 +USBP4 <-> +USBP4
19 -USBP5 <-> -USBP5
19 +USBP5 <-> +USBP5

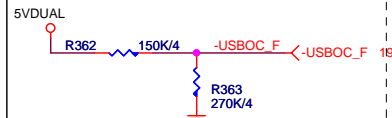


FRONT USB4

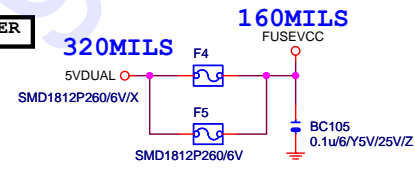
19 -USBP10 <-> -USBP10
19 +USBP10 <-> +USBP10
19 -USBP11 <-> -USBP11
19 +USBP11 <-> +USBP11



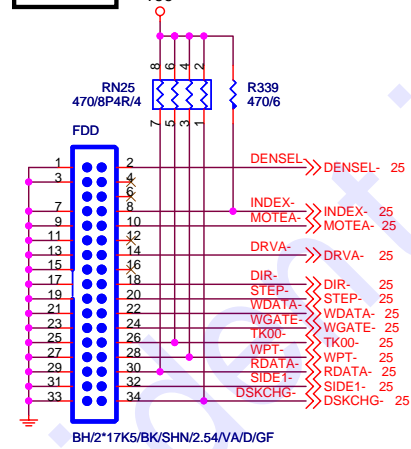
FRONT USB OC1



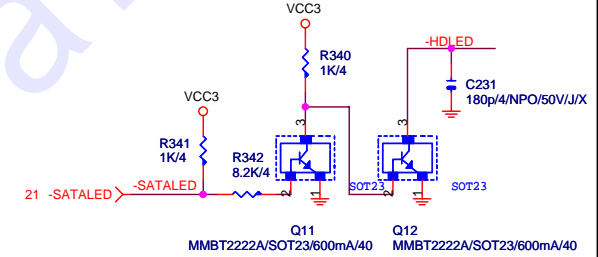
USB POWER



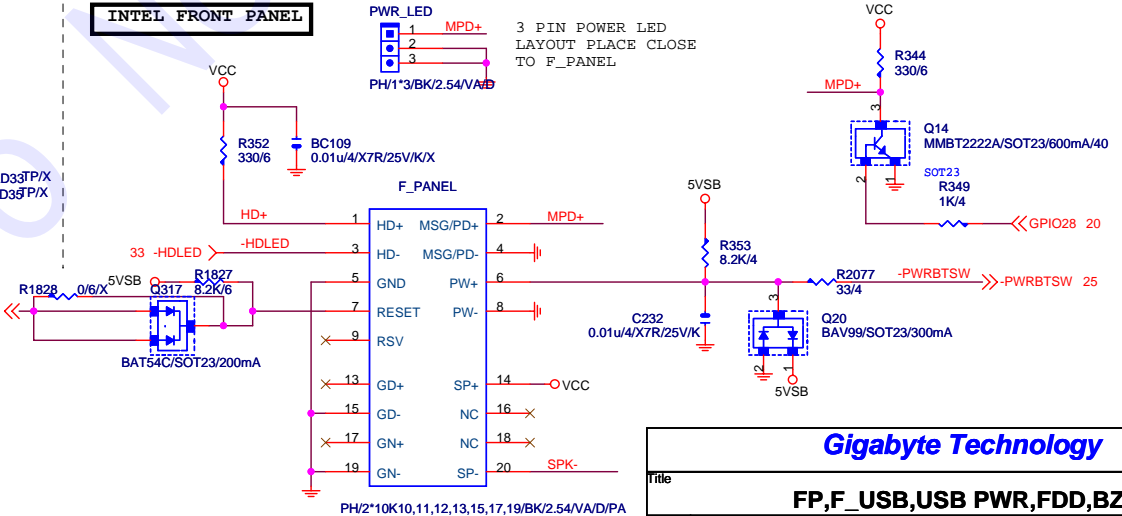
FLOPPY



SATA LED



INTEL FRONT PANEL



Gigabyte Technology

Title		FP,F_USB,USB PWR,FDD,BZ	
Size	Document Number	P35-S3	
Custom		Rev 1.02	
Date:	Wednesday, August 15, 2007	Sheet	35 of 35